80-100-193
Issue 5, September 1999

MODEL STS 5400

DS1/(E1) SYNCHRONIZATION TIMING SYSTEM

VOLUME 1

System Description

This practice applies to the following equipment:

Model	Equip Issue	Model	Equip Issue
5400-3	1	5405-9	1
5400-3A	1	5406-0	4
5400-4	3	5407-2	6
5401-1	1	5408-1	3
5402-3	3	5409-2	1
5402-4	3	5409-3	1
5403-3	3	5409-4	1
5403-4	4	5410-2	1
5404-3	4	5412-2	1
5405-4	5	5413-0	3
5405-5	3	5413-1	3
5405-8	1		

Larus Corporation
1560 Berger Drive, San Jose, CA 95112 (408) 494-1500

80-100-193A1
Issue 1, March 2001

This addendum applies to the following equipment:
Model 5410-3, Equip Issue 1
Model 5412-3, Equip Issue 1

Addendum A1

MODEL STS 5400

DS1/(E1) SYNCHRONIZATION TIMING SYSTEM

VOLUME 1

System Description

---

1. This addendum to the Model STS 5400 Volume 1, Larus Manual 80-100-193, Issue 5, calls attention to new and updated equipment issue numbers as follows:

5402-5	1
5402-6	1
5403-5	3
5403-6	4
5407-3	1
5410-2	3
5410-3	1
5412-3	1

2. Paragraph 3.3103 is amended to read as follows:

3.3103 Provisioning:

Model 5410-2 supports the AB input architecture.
Model 5410-3 is identical to the 5410-2 with the exception that the 5410-3 supports the NTS (Network Time Server) feature.
The AA architecture is not supported by the 5410 product.

3. Paragraph 3.3113 is amended to read as follows:

3.3113 Provisioning:

Model 5412-2 supports the AB input architecture.
Model 5412-3 is identical to the 5412-2 with the exception that the 5412-3 supports the NTS feature.
The AA architecture is not supported by the 5412 product.

Addendum 2

MODEL STS 5400

DS1/E1 SYNCHRONIZATION TIMING SYSTEM

VOLUME 1

System Description

---

1. This addendum applies to Larus Manual 80-100-193, Issue 5.

2. This system is normally installed in the telephone central office equipment room. In such an environment, central office battery plants can supply virtually unlimited current which is fused at the relay rack fuse panel. The installer must be aware that, when a Larus system is powered up altogether in one instant, the transient in-rush current is significant.

3. In a few customer installations, the central office battery plant is not available so a lab-type DC power supply may need to be used. Many of these DC supplies have current limiting which can be set by the user. If the current limit is set below the required in-rush current at turn on, damage to the Larus system can occur.

4. The user must ensure sufficient current is available to support the in-rush current at startup. The in-rush current requirement for some timing products at 48 Vdc can be as high as 10 amperes. Larus recommendation is that current limiting on current-limited supplies be set at 15 amperes.

Contents

Contents (continued)

Contents (continued)

Figures

Figures (continued)

Figures (continued)

Tables

[This page is intentionally left blank.]

Introduction 1

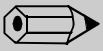
1.1 General

1.11 This document is Volume 1 of this practice series and describes the Larus Model STS 5400 Synchronization Timing System and its theory of operation. The STS 5400 is shown in Figure 1-1. This volume is intended for planners, engineers, and general users.

Installation and operation information for the STS 5400 relating to planning and engineering may be found in Volume 2, Practice 80-600-193. It describes wiring, switch settings, testing, maintenance, and troubleshooting of the STS 5400, and is intended for use by field support engineers, technicians, and craft personnel.

Volume 3, Practice 80-802-193, the Model 5405 Information Management Card Transaction Language 1 (TL1) User Manual, provides a discussion of the transaction language used by the STS 5400. It also covers performance monitoring, parameter descriptions, and security commands, and is intended for use by Control Center personnel. It is recommended that the TL1 operator read this practice in its entirety before using the STS 5400.

Volume 4, Practice 80-801-193, the Model 5405 Information Management Card Menu User Manual, provides a discussion of the menu-based user interface to the STS 5400. It also covers performance monitoring, parameter descriptions, and security commands, and is intended for use by Control Center personnel. It is recommended that the Menu operator read this practice in its entirety before using the STS 5400.



NOTE:

The STS 5400 is provisioned at the factory with either the TL1 or menu user interface.

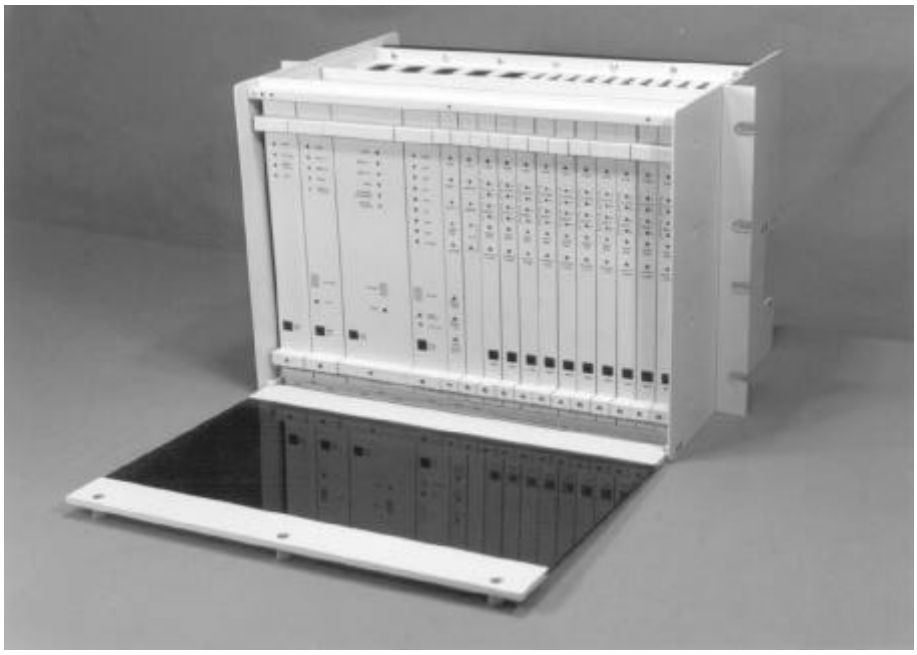


Figure 1-1.Model STS 5400 Synchronization Timing System

1.12 This practice is being reissued to include the following changes:

Model 5405 Information Management Card Lists 6 and 7 upgraded to Lists 8 and 9.
AA input architecture option discontinued for Model 5410 and 5412 GPS track and hold cards.
Previous GPS receiver replaced and corresponding 5410 and 5412 cards upgraded to List 2.
Figure 3-3, the Model STS 5400 Clock State Diagram, added.
Callouts (DS1, External Reference) corrected in Figure 5-4 and External Reference LED added to paragraph 5.427.
"Ovenized" designation for the rubidium oscillator removed in Figures 5-5 and 5-14 and paragraphs 5.524 and 5.1324.
Figure 5-13 replaced to provide a more accurate GPS mode algorithm.
Paragraphs 5.14211 and 5.14212 inserted in the Model 5412 circuit description.
Figure 5-16 modified to add the monitor and frame ground.

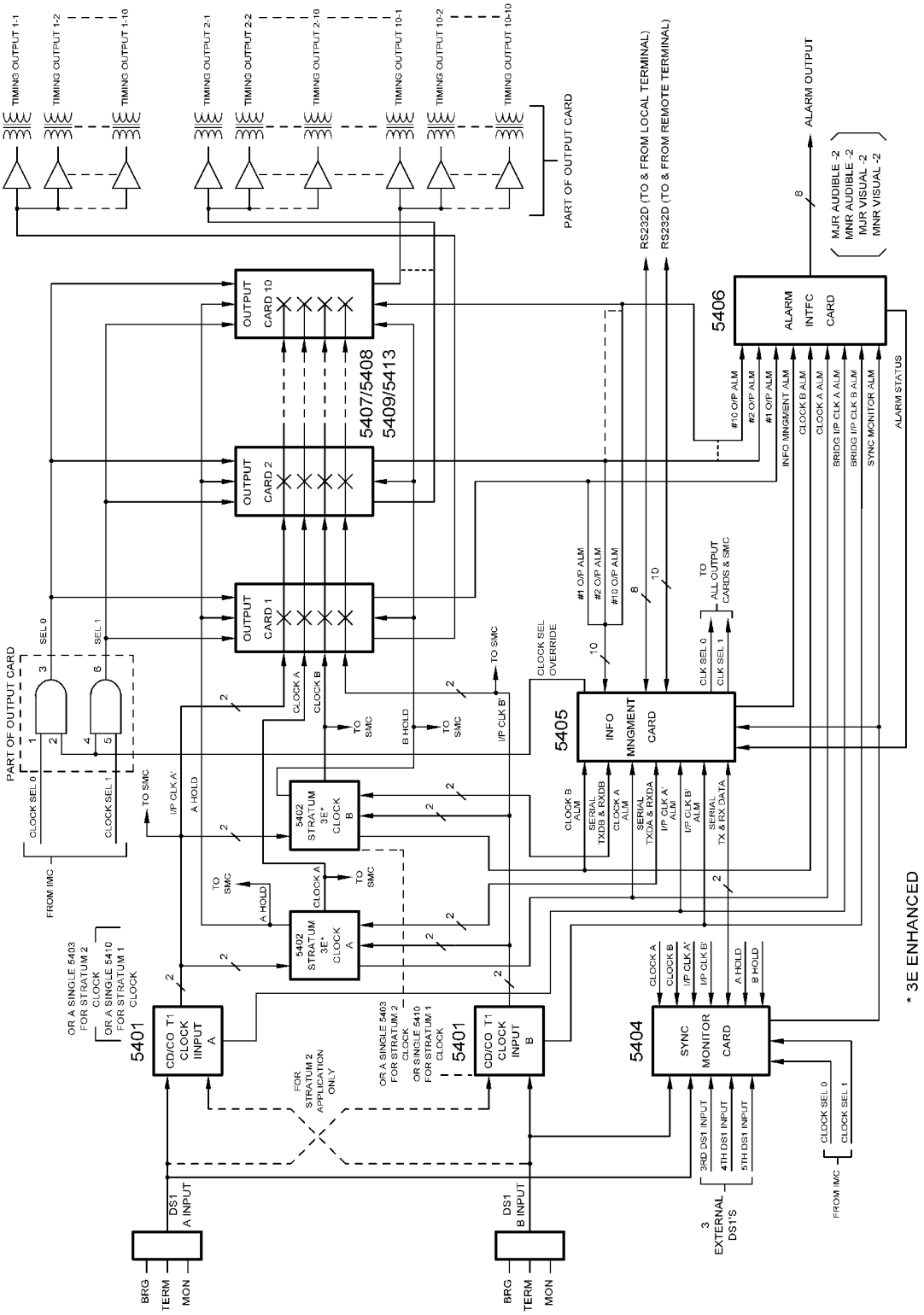
Practice Issue 5 applies to equipment referenced in Equipment Issue Information, Section 7.

1.13 The Model STS 5400 is a card family system, packaged in a Network Equipment Building System (NEBS) compatible Larus STS 5400 19/23 inch rack mounting shelf. The rack shelf contains a backplane that receives all source signals and distributes them to the appropriate cards for processing. The processed signals from the cards are delivered to the appropriate pins or connectors on the shelf backplane. The STS 5400 system block diagram is shown in Figure 1-2.

1.2 System Description

1.21 The STS 5400 provides an accurate and reliable way to synchronize communication network elements (NEs) throughout a building and, with the use of additional equipment, throughout a communication network. By synchronizing all the equipment, especially switching and multiplexing NEs, across a network, a user can maximize the utilization of network equipment and minimize network transmission errors.

1.22 Model STS 5400 systems contain one or two track and hold cards. If there are two, they must be of the same stratum level. Each of these cards contains a digital frequency synthesizer whose output is available for use by output driver cards to produce timing signals for other pieces of network equipment. Each digital frequency synthesizer uses a 10 MHz reference. The 10 MHz reference comes from an on-board oscillator, either ovenized crystal or rubidium depending on the stratum level, or an external input. The digital frequency synthesizer is made to follow or "track" an input reference by comparing the output with the input and making suitable correction to the frequency synthesizer.



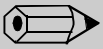
NOTE: A 5412 Stratum 1 Clock may be substituted for a 5402 Stratum 3E Enhanced Clock.

Figure 1-2. Model STS 5400 System Block Diagram

1.23 In Stratum 1 systems, the input tracking reference is derived from a set of cesium beam atomic clocks aboard orbiting Global Positioning System (GPS) satellites whose signals are transmitted to an on-board GPS receiver. As a result, external input references are not required for normal operation. However, the Stratum 1 track and hold cards do have tracking reference inputs to permit them to be operated as Stratum 2 or 3E Enhanced cards, depending on the model, if there is a GPS failure.

1.24 A GPS failure could be caused by damage to the external GPS antenna, damage to the cabling between the GPS antenna and the STS 5400 shelf, or failure of the on-board GPS receiver itself. The U.S. Department of Defense, which operates the GPS satellite system, has the ability to add variable amounts of jitter to the GPS timing signals. The jitter, known as selective availability (S/A), is intended to hinder an enemy's attempt to use the GPS system in times of national threat. Excessive amounts of S/A can also cause a GPS failure.

1.25 The Stratum 2 and 3E Enhanced systems (and Stratum 1 with GPS failure) use external signals as tracking references. Track and hold cards at each stratum can acquire and track signals that meet the requirements of the same or lower (more precise) stratum. Normally, Digital Signal Level 1 (DS1) signals traceable to a Stratum 1 source should be used. The output of an STS 5400 Stratum 2 or 3E Enhanced system that has references from Stratum 1 sources will meet the Stratum 1 requirements.



NOTE:

Stratum 3E Enhanced is the designation for the clock system devised by Larus Corporation that improves on the standard Stratum 3E as defined in Bellcore documents. Refer to Section 2, Table 2-A.

1.26 Each track and hold card has provision for two DS1 tracking reference inputs, one primary and one secondary, and contains circuitry to remove jitter and wander from the DS1 input being tracked. If an STS 5400 system loses its active tracking reference, the cards switch to holdover mode where the digital frequency synthesizer continues to run at the last setting before the reference was lost. Frequency accuracy in holdover determines the stratum level of the various track and hold card models. After a track and hold card switches into holdover mode, it attempts to acquire and track the reference signal at its secondary tracking input. If it is successful, the card will continue normal operation.

1.27 Two input architectures are available for STS 5400 systems with two 5402 or 5403 track and hold cards. The AA input architecture has both cards using the same source as the primary DS1 tracking reference and another source for the secondary DS1 tracking reference. The AB input architecture uses one source as primary on one card and the other source as secondary. The other card reverses the references so that each DS1 source is primary on one track and hold and secondary on the other. The 5410 and 5412 track and hold cards provide only the AB input architecture.

1.28 The AA architecture has this advantage if there is a failure of the input track and hold card being used by the output driver cards: when the output driver cards switch to use the output from the other track and hold card there should be minimal phase change in the outputs of the output driver cards. However, if there is a failure of the primary reference source, both input track and hold cards will go into holdover mode which is less accurate than tracking mode. The cards will then attempt to acquire and track the secondary DS1 reference. This could cause some phase change as the track and hold cards change input references.

1.29 The advantage of the AB architecture is that, with two input track and hold cards each tracking a different DS1 reference, there is very little chance that both cards would go into holdover mode at the same time. There would need to be a multitude of failures to allow the STS 5400 to produce output signals that are not referenced to an input.

1.210 In either case, the STS 5400 track and hold cards have phase alignment circuitry that causes the secondary card to attempt continually to align its output phase with the primary card, regardless of the reference being tracked. Thus, an input switch by the output driver cards from one input track and hold card to the other will cause a minimal phase change at the outputs.

1.211 The STS 5400 is nonrevertive which means that, if the primary DS1 reference fails and the track and hold card(s) switches to use the secondary DS1 input, the card(s) will not switch back to use the primary DS1 input unless the secondary input fails.

1.212 As another alternative, the STS 5400 track and hold cards can be commanded to use an external 10 MHz source as a tracking reference. A suitable external 10 MHz source could come from a cesium beam clock, a GPS receiver, a LORAN-C receiver, or similar precision source. The accuracy of the outputs from an STS 5400 in this configuration is related to the accuracy of the external 10 MHz source.

1.213 If a track and hold card has never been in tracking mode since it was powered up, there is no information available to set the frequency synthesizer for holdover mode. In this case, the frequency synthesizer is set to run at the nominal default frequency. This mode is called free run. Since there is no reference available to compare to the output frequency in free run, the output frequency could be farther off-frequency than in holdover.

1.214 Each of the output driver cards can select from four inputs, one from each of the input track and hold cards and one from each DS1 input reference directly. Logic on each output driver card selects the "best" timing source. A timing signal from a track and hold card that is tracking an input reference is "better" than a timing signal from a card that is in holdover. By the same token, a timing signal from a track and hold card in holdover mode is "better" than a DS1 reference input. If at any time a "better" signal source than the one in use becomes available, the output driver cards will switch to use the better source. The output driver cards contain circuitry to limit the rate of output phase change after a switch. The first track and hold card to achieve tracking mode is selected as the primary card. Circuitry on each output driver card causes all output cards to select the same timing reference as the leftmost output driver card in the shelf. Each output driver card produces ten outputs.

1.215 The STS 5400 contains auxiliary cards that measure the performance of the system, provide indication of hardware failures, and furnish command and status interfaces to the system.

1.216 The STS 5400 provides functional fault tolerance in a number of ways, offering redundant track and hold cards with dual DS1 inputs and provision for multiple (up to ten) output driver cards, for example. Since many pieces of network equipment have two timing inputs, an output from each of two output driver cards from one STS 5400 or, better still, two different STS 5400 systems should be connected.

1.217 Another feature is individual DC-to-DC converters on each card. This removes a common power supply as a single point of failure. Failure of one DC-to-DC converter affects only one card. Critical components like the track and hold and output driver cards can be redundant so that a failure of one does not cause a loss of service in the network equipment.

1.218 Failure of an auxiliary card does not affect the primary system function, which is to produce accurate timing signals.

1.219 Failures are categorized into major, indicating a loss of service, and minor, indicating a loss of function. The STS 5400 provides means whereby major and minor alarms can be connected to indicators to summon service personnel for timely repair.

1.3 Versions

The STS 5400 can accept either one or two framed DS1 signals as input references. From these and other inputs, timing is extracted and used to discipline the oscillator on each clock card. The Larus STS 5400 system is available in three versions: Stratum 3E Enhanced, Stratum 2, and Stratum 1.

1.31 Stratum 3E Enhanced System (Stratum 3E Central Clock)

A redundant STS 5400 Stratum 3E Enhanced system requires a 5400-3A (non-GPS) or 5400-4 (GPS) mounting shelf with backplane, two 5401 Input Cards, two 5402-3 or 5402-4 Stratum 3E Enhanced Track and Hold cards, equipped with crystal oscillators, and up to ten output driver cards consisting of any mix of DS1 (5407-2), Composite Clock (5408-1), European Standard (E1) all ones (5409-2or 5409-4), E1 Square Wave (5409-3), 1.544 MHz EIA RS-422 Square Wave (5413-0), and 8 kHz EIA RS-422 Square Wave (5413-1) cards. Figure 1-3 shows the front panel layout of a fully equipped Stratum 3E Enhanced system.

The 5402-3 Stratum 3E Enhanced Track and Hold Card provides the AB input architecture. The 5402-4 provides the AA input architecture.*

* The AA versus AB input architecture is described in Appendix A.

1.32 Stratum 2 System (Stratum 2 Central Clock)

A redundant Stratum 2 system comprises either a 5400-3 (non-GPS) or 5400-4 (GPS) mounting shelf, and substitutes a 5403-3 or 5403-4 Stratum 2 Track and Hold Card, equipped with a rubidium oscillator, for each of the two 5401/5402 pairs in a 3E system. The mix of output driver cards is the same as listed above. Figure 1-4 shows the front panel layout of a fully equipped Stratum 2 system.

The 5403-3 Stratum 2 Track and Hold Card provides the AB input architecture. The 5403-4 provides the AA input architecture.

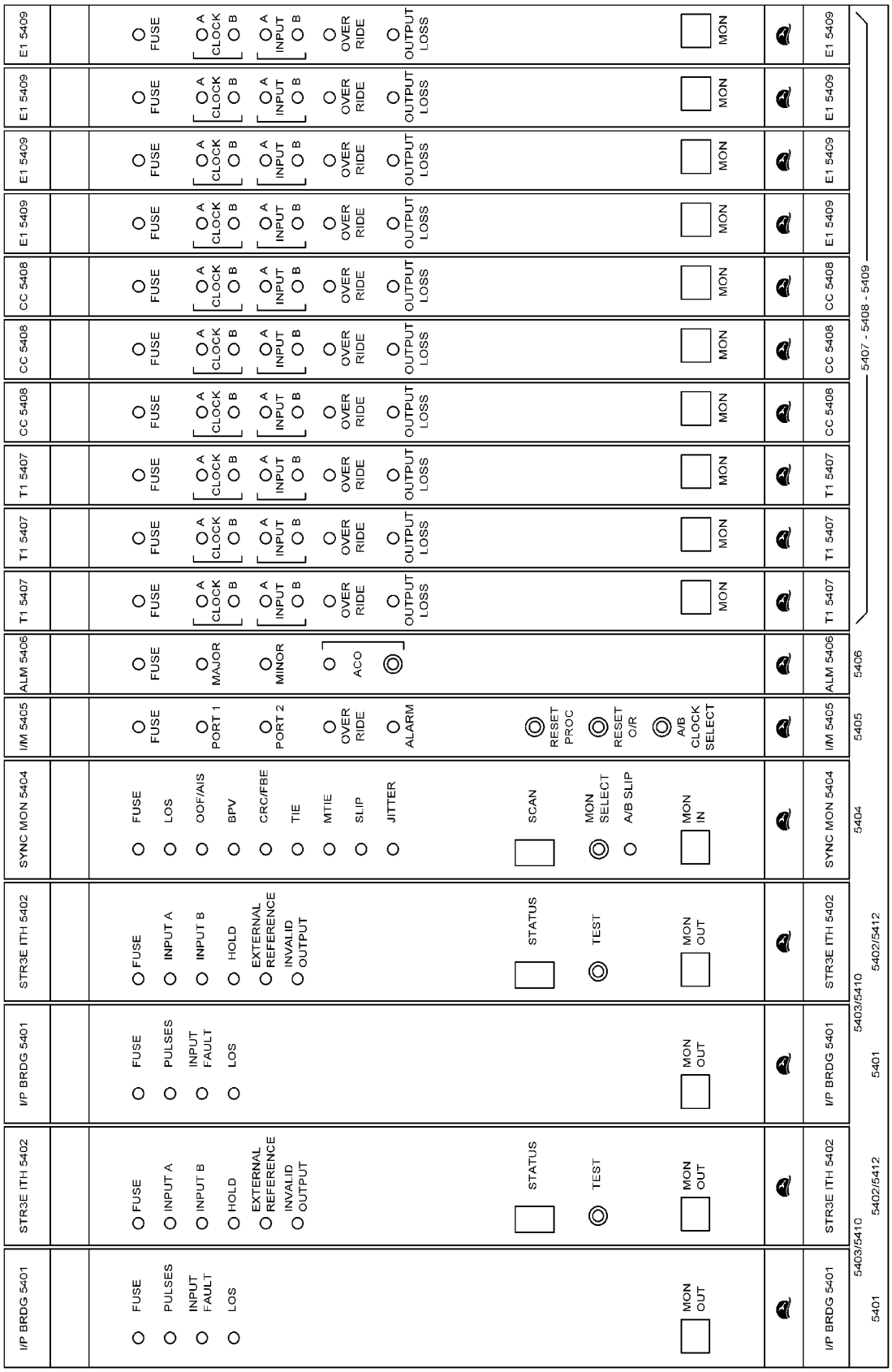


Figure 1-3. Model STS 5400 Front Panels, Stratum 3E Enhanced (5402)

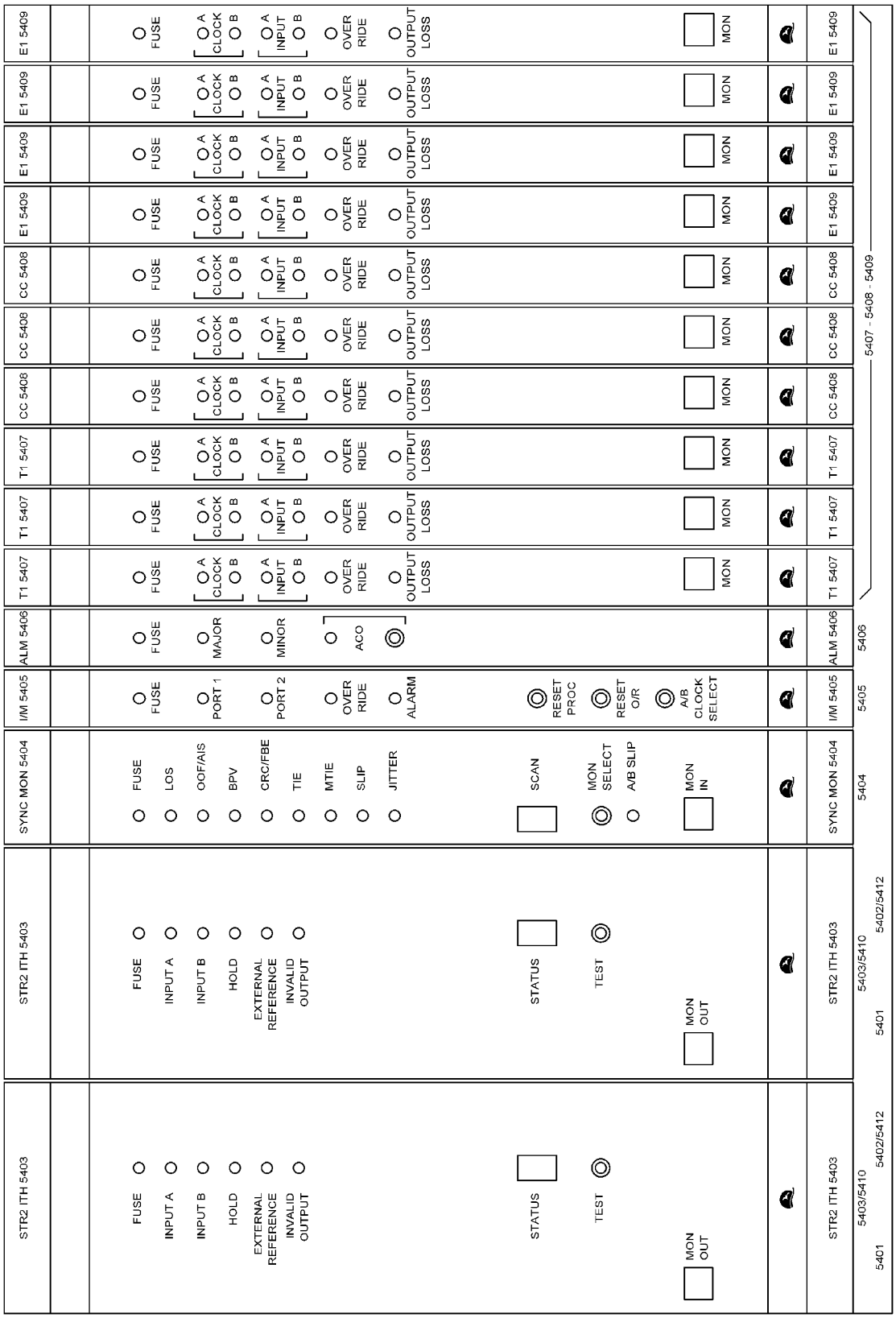


Figure 1-4. Model STS 5400 Front Panels, Stratum 2 (5403)

1.33 Stratum 1 System

A redundant Stratum 1 system uses a 5400-4 shelf, and substitutes a 5410-2 GPS Stratum 1 Track and Stratum 2 Hold Card for each 5403 Stratum 2 Track and Hold Card or a 5401 Input Card and 5412-2 GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card for each of the two 5401/5402 pairs. Figure 1-5 depicts the front panel of a Stratum 1 system equipped with 5410 cards. Figure 1-6 shows the front panel layout of a Stratum 1 system equipped with 5412 cards.

The 5410-2 and 5412-2 provide the AB input architecture. The AA input architecture is not supported.

Additional Information on 5410 and 5412 Cards

The 5410 and 5412 cards incorporate a GPS receiver and timing processor. The receiver normally requires a rooftop antenna to furnish adequate signal strength for dependable reception and tracking. The antenna should be located for the 'best view of the sky.' The antenna cable connects to the rear of the STS 5400-4 shelf at the GPS antenna connector. Inside the shelf, the coax is routed to the GPS receiver unit within the 5410/5412 card.

Standard antenna kit:

GPS antenna (weatherproof and less than 5 inches in height)
Normal surface mounting and pole mounting bracket with hardware
50 feet of RG-58 coaxial cable with connectors

In general, GPS uses a sophisticated technology which simultaneously tracks signals from multiple nongeostationary communications satellites. The U.S. military originally mandated this global system primarily for precision navigation. Its secondary role is that of an accurate frequency source. The U.S. military maintains daily calibration of the primary frequency reference [an atomic clock traceable to Coordinated Universal Time (UTC)] in each healthy satellite; however, it also retains the right to use the S/A mode to force a temporarily increased error factor for navigational as well as frequency purposes. It is designed to prevent hostile forces from using the GPS effectively.

(continued)

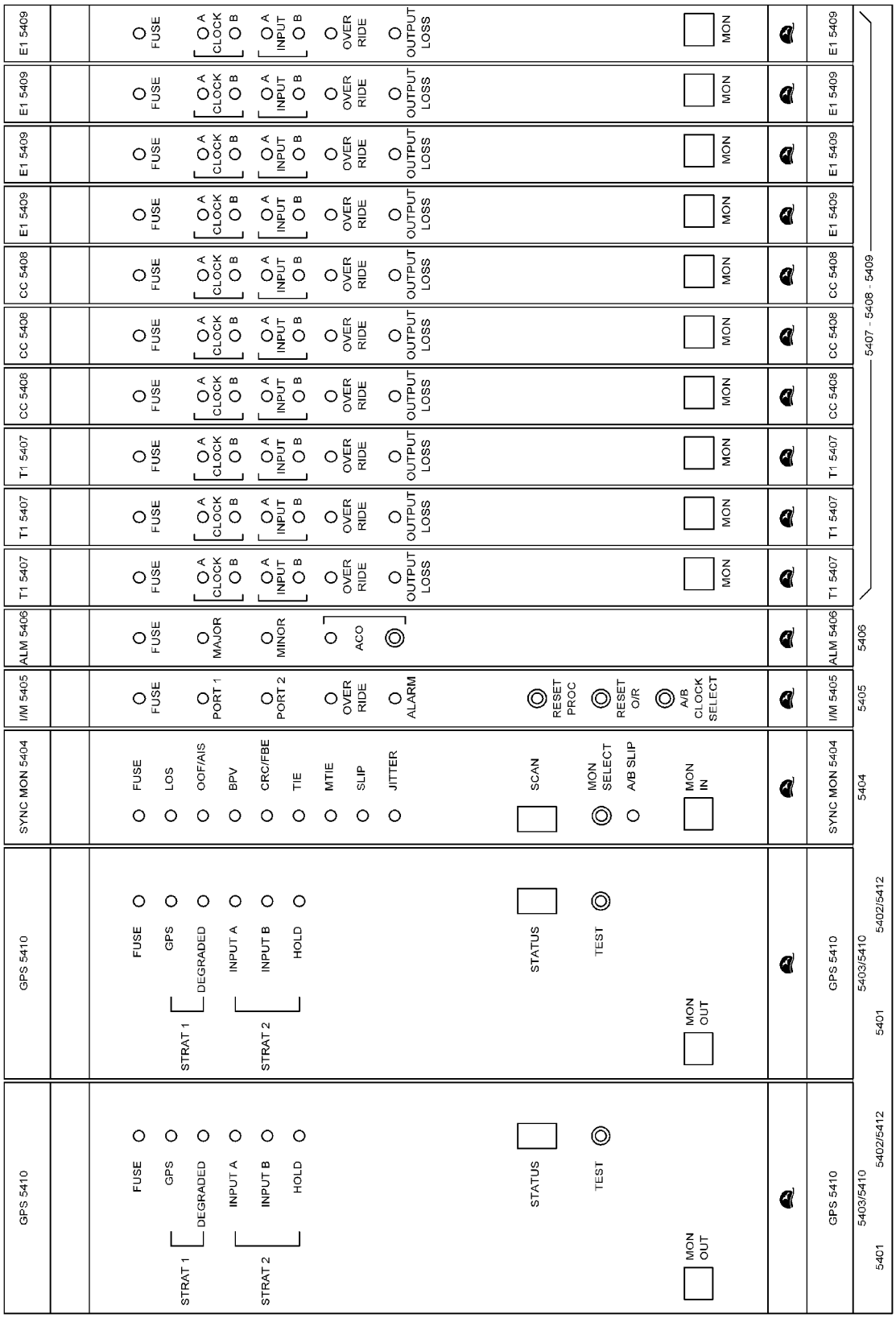


Figure 1-5. Model STS 5400 Front Panels, Stratum 1/2 (5410)

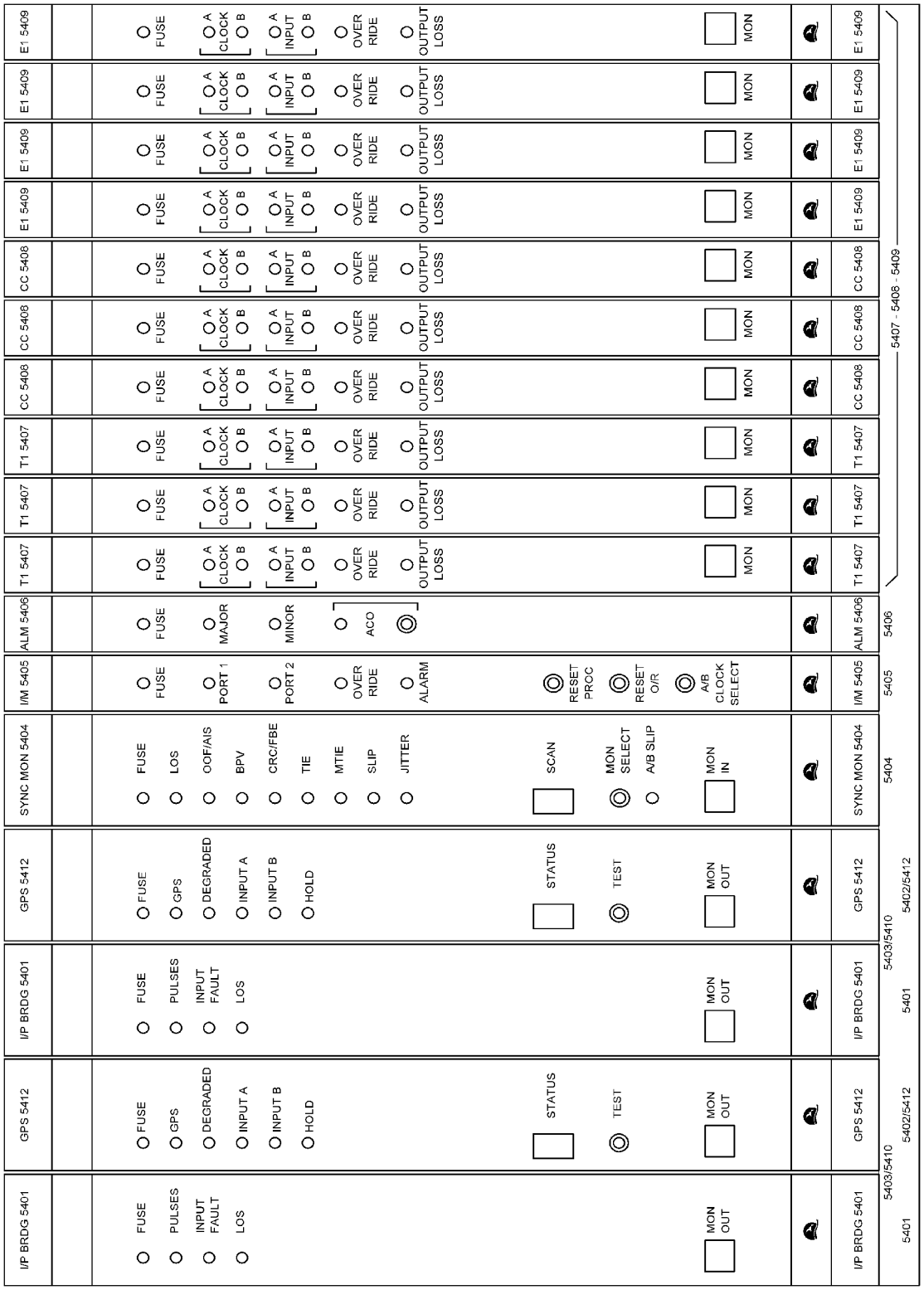


Figure 1-6. Model STS 5400 front Panels, Stratum 1/3E (5412)

1.33 (continued)

The GPS radio receiver internal to the Larus 5410/5412 module receives and compares signals from these satellites and processes a result, not in terms of a precise location but in terms of a precision frequency, since it assumes that the installation has a fixed location on earth. It tracks eight or more satellites in the sky and can use signals from at least three satellites to triangulate a location, with a fourth satellite to check on the first three. Using the fourth, it can calculate and compensate for clock error by solving four simultaneous equations (one for each satellite measurement). The output of the GPS radio receiver, a stable reference of exactly one pulse per second (1PPS), is then used by the Precision Time Assembly. The Precision Time Assembly compares this 1PPS with the on-board frequency reference of the 5410/5412 to develop a time correction factor.

A GPS failure can be caused by damage to the GPS antenna or cable. In addition, the U.S. Department of Defense may increase the amount of S/A jitter transmitted by the satellites in times of heightened national threat. Excessive amounts of S/A jitter cause loss of GPS tracking. The 5410 includes a rubidium oscillator for Stratum 2 Hold performance in the event of loss of the GPS primary reference. The 5412 includes an ovenized crystal oscillator for Stratum 3E performance in Hold in the event of loss of GPS tracking. The internal oscillators allow the 5410 and 5412 to ignore short-term GPS tracking loss.

1.34 Track and Hold Card Combinations

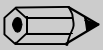
The following combinations of track and hold cards are acceptable:

Stratum 1 (GPS) with Stratum 2 Hold:	Two 5410-2* cards, or One 5410-2* and one 5403-3* card
Stratum 1 (GPS) with Stratum 3E Enhanced Hold:	Two 5401 and two 5412-2* cards, or Two 5401 cards, one 5412-2* and one 5402-3* card

1.34 (continued)

Stratum 2:	Two 5403-3* or 5403-4** cards
Stratum 3E Enhanced:	Two 5401 and two 5402-3* or 5402-4** cards

* Provides AB input architecture.
** Provides AA input architecture.



NOTE:

Track and hold cards in any combination must provide the same input architecture, whether AA or AB.

Systems that have AA architecture have both input track and hold assemblies tracking the same input.

Systems that have AB architecture have each input track and hold assembly tracking a different input.

Refer to Appendix A for a detailed description of AA and AB input architecture.

1.35 Characteristics Common to All Systems

Each output driver card provides ten outputs so that the maximum number of outputs for the shelf is 100. These can be arranged in 50 redundant pairs (even and odd) so that, if any one output fails, the other output of the pair will still be valid. Alarm and status reporting, performance monitoring, and operation support system (OSS) interface is provided by the 5404, 5405, and 5406 cards.

1.4 Cards

NOTE:

A complete description of each STS 5400 circuit card is presented in Section 5 of this Volume.

1.41 More than a dozen cards can be used in the STS 5400 timing system. The cards plug into a rack shelf backplane to receive inputs from the source system. The cards also deliver their output signals to connectors and pins on the backplane. Refer to Table 1-A for card function and identification.

1.42 The system uses from one to ten output driver cards. These are available for 64/8 kHz Composite Clock, DS1, E1, 2.048 MHz square wave, 1.544 MHz EIA RS-422 square wave, and 8 kHz EIA RS-422 square wave outputs. As mentioned above, each card provides ten outputs, allowing up to 100 outputs from one shelf.

1.43 Each system also uses performance monitor and alarm reporting cards, comprised of the 5404 Synchronization Monitor Card, the 5406 Alarm Interface Card, and the 5405 Information Management Card. In general, alarms are reported by front panel light emitting diode (LED) indicators, by relay contact closures on the 5406 card, and by alarm messages from the 5405 card to an OSS or local craft terminal.

NOTE:

An input jack is provided on the front panel of the 5404 card. The bantam size (–20 dBsx signal level) permits the fifth DS1 input signal to be received via front panel access.

1.44 The Larus Model STS 5400 offers a fully redundant wander- and jitter-free source of framed ones, composite clock, or square waves synchronized to a suitable framed DS1, 10 MHz, or GPS atomic time reference. Jitter and wander attenuation is a standard function of the track and hold cards. The 5400 timing system provides inputs for two DS1 references, two 10 MHz references, and two GPS antenna connections.

Table 1-A

Card Function and Identification

Function	Model
DS1 Bridging Input Card	5401-1
Stratum 3E Enhanced Track and Hold Card	5402-3 (AB) or 5402-4 (AA); requires a 5401-1 DS1 Input Card
Stratum 2 Track and Hold Card	5403-3 (AB) 5403-4 (AA)
Synchronization Monitor Card	5404-3
Information Management Card [Transaction Language Number 1 (TL1) Interface Software]	5405-8 (AB) 5405-4 (AA)
Information Management Card (Menu Control Interface Software)	5405-9 (AB) 5405-5 (AA)
Alarm Interface Card	5406-0
DS1 Output Driver Card (10 outputs)	5407-2
Composite Clock Output Driver Card (10 outputs)	5408-1
E1 Output Driver Card (10 outputs)	5409-2
2.048 MHz Square Wave Output Driver Card (10 outputs)	5409-3
E1 Output Driver Card with Multiframe Synchronization for CAS or CRC4 (10 outputs)	5409-4
GPS Stratum 1 Track and Stratum 2 Hold Card (includes antenna kit)	5410-2 (AB)
GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card (includes antenna kit)	5412-2 (AB); requires a 5401-1 DS1 Input Card
EIA RS-422 Output Driver Card (10 outputs)	5413-0 (1.544 MHz) 5413-1 (8 kHz)

Note: Hyphen denotes List option (e.g. 5408-1 is 5408 List 1).

1.45 The average bit rate of the DS1 input references must be in the range of 1.544 Mbps ±7.1 bps for Stratum 3E Enhanced or 1.544 Mbps ±0.04 bps for Stratum 2 oscillators to "pull-in" and track.

1.46 For redundant Stratum 3E Enhanced and 2 systems, two digitally controlled frequency synthesizers (one in each 5402 or 5403 card) track the separate DS1 framed input reference signals while the inputs are within the above frequency limits. For the Stratum 1 systems, the digitally controlled frequency synthesizers are adjusted to compensate for drift relative to the GPS atomic time.

1.47 The frequency synthesizers initially operate in the acquire mode, attempting to adjust their frequency to bring the phase error relative to the reference input to zero. When the phase error is relatively small, the frequency synthesizers shift into the tracking mode.

1.48 If a reference input is lost, the frequency synthesizer continues with the last known frequency settings and signals the output cards that it is in holdover. The output cards switch to use the track and hold output that is still tracking. After a short period of time, the track and hold card will switch to attempt to acquire the secondary input reference. If the secondary input is within the pull-in tolerances, the frequency synthesizer will be able to track it and switch out of holdover mode.

1.49 If both inputs are lost, the track and hold card will stay in holdover mode. Typical performance is less than one frame slip in 36 hours for the Stratum 3E Enhanced track and hold cards and two months or more for the Stratum 2 track and hold cards.

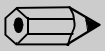
1.410 There is also a free running mode where the frequency synthesizer runs at its nominal center frequency. The track and hold cards will automatically enter the free run condition after a prescribed time without a suitable input reference. The oscillators can also be put in free run for testing. If both cards fail, the system will use either input (if good) to drive the outputs directly. If both track and hold cards and both inputs fail, all outputs are suppressed.

1.5 Features

1.51 Unless otherwise noted, the features listed below apply to all versions of the 5400 system:

a. Redundant DS1 or E1 framed all ones; 8 kHz, 1.544 MHz, or 2.048 MHz square wave; or 64/8 kHz composite clock outputs synchronized to a framed DS1 or 10 MHz reference source.

b. Hitless switching from primary track and hold card to secondary card in the event of an input reference failure, to assure that all outputs are driven by a track and hold card tracking a valid signal.



NOTE:

Refer to the description of phase alignment in Appendix B.

c. In the event that both inputs fail (HOLD state), output frequency held to less than four DS1 frame slips in the first 24 hours, worst case, for Stratum 3E Enhanced. For Stratum 2, the time to the first frame slip is about seven days and for Stratum 1 it is 72 days.

d. Flexible architecture. In the minimum configuration, one input card may be used with one track and hold and one output card in a non-redundant system. In a maximum configuration, up to 100 outputs are available from the shelf.

e. Wander and jitter attenuation in compliance with Bellcore TR-NWT-000499.

f. Clock tracking algorithms with relatively fast acquisition times for power-up and return from the HOLD state. After the signal is acquired, a slower tracking state is entered to provide attenuation of wander with settling times of 3000 seconds (Stratum 3E Enhanced) or 10,000 seconds (Stratum 2).

g. Compliance with Bellcore TA-TSY-000378, Bellcore TA-NPL-000436, AT&T PUB 60110, ANSI*/T1.101-1994, and CCITT G.703-1988.

* Registered trademark of the American National Standards Institute, Inc.

(continued)

1.51 (continued)

h. Frequency tracking to ±7.1 Hz (Stratum 3E Enhanced) or ±0.04 Hz (Stratum 2).

i. Frequency accuracy of 1 x 10^{-11} for Stratum 1 per Bellcore GR-1244-CORE.

j. Invalid input signal detection by 5401 Input Cards, 5402, 5403, 5410, or 5412 Track and Hold Cards, and 5404 Synchronization Monitor Card.

k. Floating alarm contacts provided by the 5406 Alarm Interface Card: Major (loss of both sources of input synchronization or any other condition providing loss of one or more output pairs) and Minor (loss of any one input or any one output).

l. Performance monitoring, including time interval error (TIE), maximum time interval error (MTIE), wander and jitter of the two reference inputs and any of the three external DS1 signals, provided by the 5404 Synchronization Monitor Card. Terminating, bridging, and monitor inputs are provided for each of the five DS1 input signals.

m. Status, performance, and alarm reporting through local and remote EIA RS-232 ports as well as remote control of oscillator mode and output selection provided by the 5405 Information Management Card.

n. Low power consumption, approximately 90 watts per shelf for a full Stratum 3E Enhanced system, 105 watts for a full Stratum 2 system, and 110 watts for a full Stratum 1 system.

o. NEBS compatible rack mounting.

1.6 Options

1.61 The options listed below apply as indicated to any or all versions of the 5400 system: Stratum 1, Stratum 2, and Stratum 3E Enhanced.

1.62 The STS 5400 system may be ordered on a card-by-card basis to obtain either a minimal system with no redundancy (not recommended) or a fully redundant system. Additional monitoring and control functions are provided by the 5404 Synchronization Monitor Card and 5405 Information Management Card.

1.63 A minimal Stratum 3E Enhanced system comprises:

One 5400-3A (non-GPS) or 5400-4 (GPS) Mounting Shelf.
One 5401-1 Input Card.
One 5402-3* or 5402-4** Stratum 3E Enhanced Track and Hold Card.
Any combination of output driver cards (up to ten) listed in paragraph 1.66.

A minimal redundant system requires two 5401-1 and two 5402-3* or 5402-4** cards.

Reference NOTE below.

1.64 A minimal Stratum 2 system comprises:

One 5400-3 (non-GPS) or 5400-4 (GPS) Mounting Shelf.
One 5403-3* or 5403-4** Stratum 2 Track and Hold Card.
Any combination of output driver cards (up to ten) listed in paragraph 1.66.

A minimal redundant system requires two 5403-3* or 5403-4** cards.

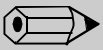
Reference NOTE below.

1.65 A minimal Stratum 1 system comprises:

One 5400-4 (GPS) Mounting Shelf.
One 5410-2* GPS Stratum 1 Track and Stratum 2 Hold Card, or one 5401-1 Input Card and one 5412-2* Stratum 1 Track and Stratum 3E Enhanced Hold Card.
Any combination of output driver cards (up to ten) listed in paragraph 1.66.

A minimal redundant system requires two 5410-2* cards or two 5401 and two 5412-2* cards for each Stratum 1 system.

Reference NOTE below.



NOTE:

*** Provides AB input architecture.**
**** Provides AA input architecture.**

Both track and hold cards in any combination must support the same input architecture, either AA or AB.

1.66 The STS 5400 output driver cards include:

5407-2	DS1 Framed All Ones
5408-1	Composite Clock
5409-2	E1 Framed All Ones
5409-3	2.048 MHz RS-422 Square Wave
5409-4	E1 Framed All Ones, CAS or CRC4
5413-0	1.544 MHz RS-422 Square Wave
5413-1	8 kHz RS-422 Square Wave

1.67 Any of the following may be added to the above listed systems:

One 5406-0 Alarm Interface Card.
One 5404-3 Synchronization Monitor Card.
One 5405-4, -5, -8, or -9 Information Management Card.

NOTE:

The 5405 Information Management Card, if present, must be provisioned with the same input architecture, AA or AB, as the track and hold cards.

Applications 2

2.1 General

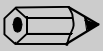
2.11 Unless otherwise stated, the applications listed below apply to all versions of the 5400 system: Stratum 1, Stratum 2, and Stratum 3E Enhanced.

2.12 The Model STS 5400 Synchronization Timing System is intended for use in either a Digital Signal Level 1 (DS1) or European Standard (E1) digital transmission environment. It is compatible with the Synchronization Plan of Bellcore TA-NPL-000436 and AT&T PUB 60110, with the Timing Signal Generator requirements of Bellcore TA-TSY-000378, and with the Synchronization Network Interface requirements of ANSI*/T1.101-1994 and CCITT G.703-1988.

* Registered trademark of the American National Standards Institute, Inc.

2.13 The Model STS 5400 provides timing for transmultiplexers, digital access and crossconnect systems (DACSs), SONET (Synchronous Optical Network) and SDH (Synchronous Digital Hierarchy, the European equivalent to SONET) equipment, digital switches, channel banks, and any other equipment requiring network synchronization. General considerations of network timing distribution and the Central Clock (BITS clock) concept are presented in subsection 2.2.

2.14 Input timing may be derived from existing traffic-bearing DS1 framed signals. The STS 5400 provides for two independent DS1 inputs. Additionally, the 5410 and 5412 cards derive their timing from an integral Global Positioning System (GPS) receiver.



NOTE:

The 5410 and 5412 GPS receivers normally require a rooftop antenna for dependable reception and tracking of the GPS satellite signals. The antenna connector is located on the rear of the STS 5400-4 mounting shelf. See Section 5, Figure 5-2.

2.15 Output signals are either framed all ones at DS1 or E1 rates and formats; 64/8 kHz composite clock; or 8 kHz, 1.544 MHz, or 2.048 MHz square wave.

2.16 The Model STS 5400 system can interface with a remote operation support system (OSS) and a local craft terminal for monitoring and control.

2.17 Figures 2-1 through 2-4 depict the Model STS 5400 system applications.

2.18 Designing the location of master and slave terminals becomes difficult when point-to-point circuits are used for add and drop services, switched services, or services passing through certain customer multiplexing equipment. However, reliable network timing can be achieved if one location is designated as the master and Stratum 2 or 3E Enhanced clock systems are installed at all other sites.

2.19 In ring systems, as is the case with many modern fiber and radio networks, using the traffic-carrying DS1 to drive the timing systems is not generally recommended but has been found to work well and solve many problems.

2.110 SONET and SDH networks are designed to operate in a maintenance mode when not timed. In this mode, the jitter may be larger than that of a properly timed network. It has been noted that for voice traffic, and even for digital traffic between switches and digital crossconnects, no impairments are observed even when the SONET system is untimed. However, it is recommended that all SONET networks be timed to minimize phase noise (jitter and wander).

2.111 With SONET, the multiplex equipment must be timed. If the timing of the dropped DS1s is different from the multiplex timing, there will be unsatisfactory jitter and wander performance which may or may not affect the connected equipment. By timing all network sources of DS1 signals from the same reference, and making sure that the reference chosen is the same as the SONET reference, problems can be minimized.

2.2 Timing Distribution and Central Clock Considerations

2.21 Synchronization Networks

2.211 Synchronization networks provide timing signals to all synchronizable network elements (NEs) at each node in a digital network. These timing signals are traceable to a highly accurate Primary Reference Source (PRS) clock. The aim is to ensure that all outgoing transmissions from a digital network node have the same average frequency. Buffer elements at important transmission interfaces absorb differences between the average local frequency and the actual short-term frequency of incoming signals which may be affected by phase wander and jitter accumulated along the transmission paths.

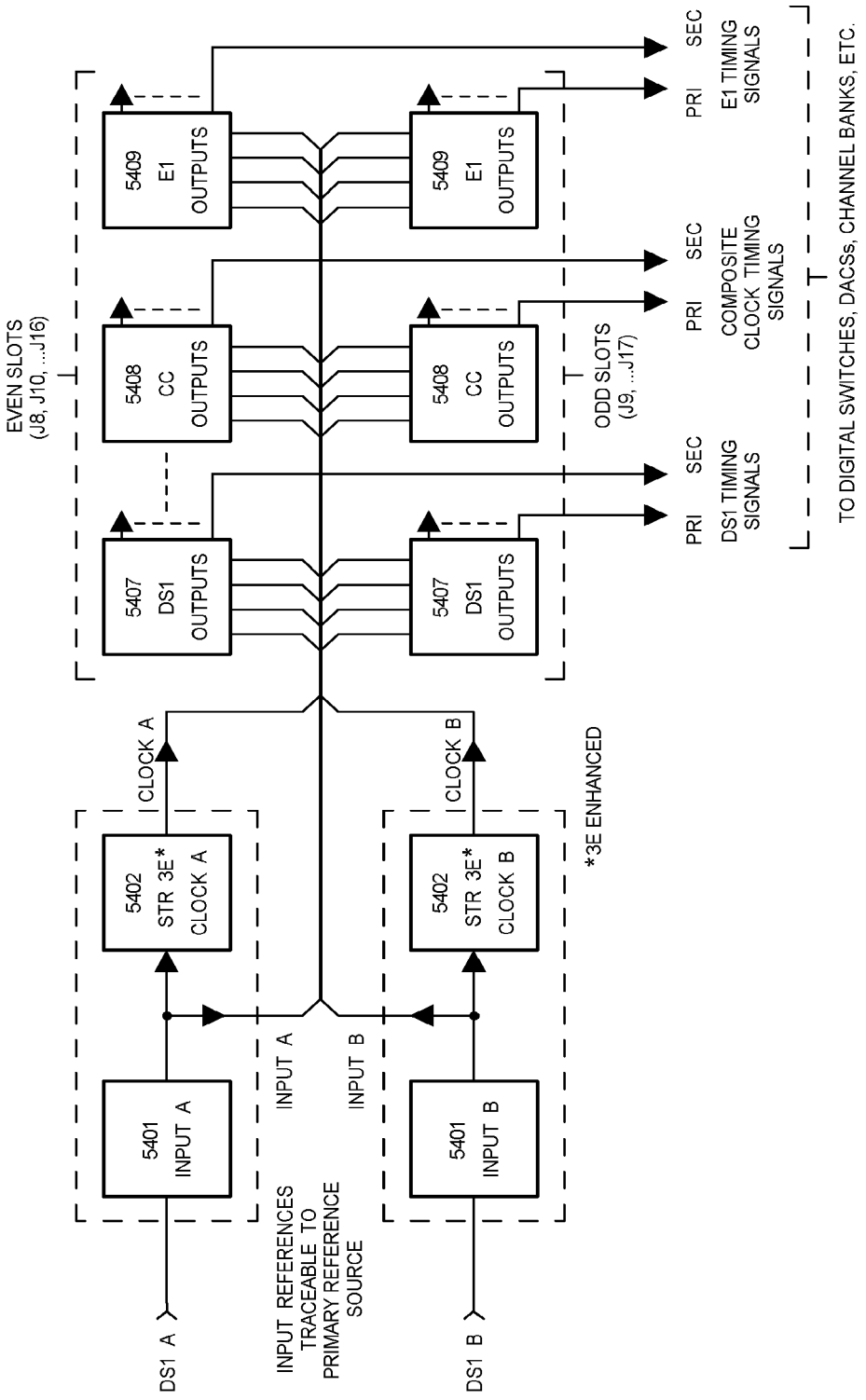


Figure 2-1. Model STS 5400 Stratum 3E Enhanced Application Diagram (5402)

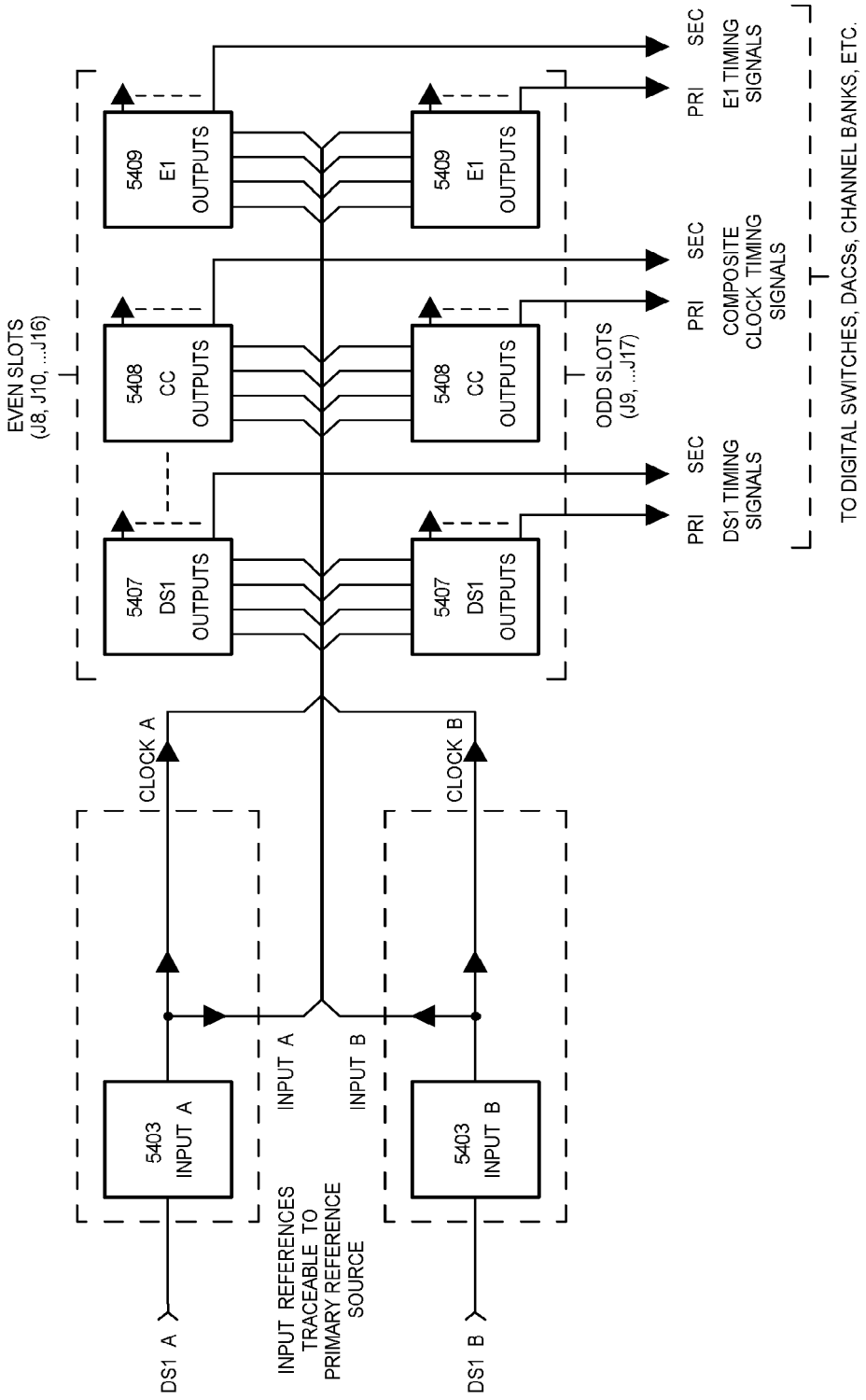


Figure 2-2. Model STS 5400 Stratum 2 Application Diagram (5403)

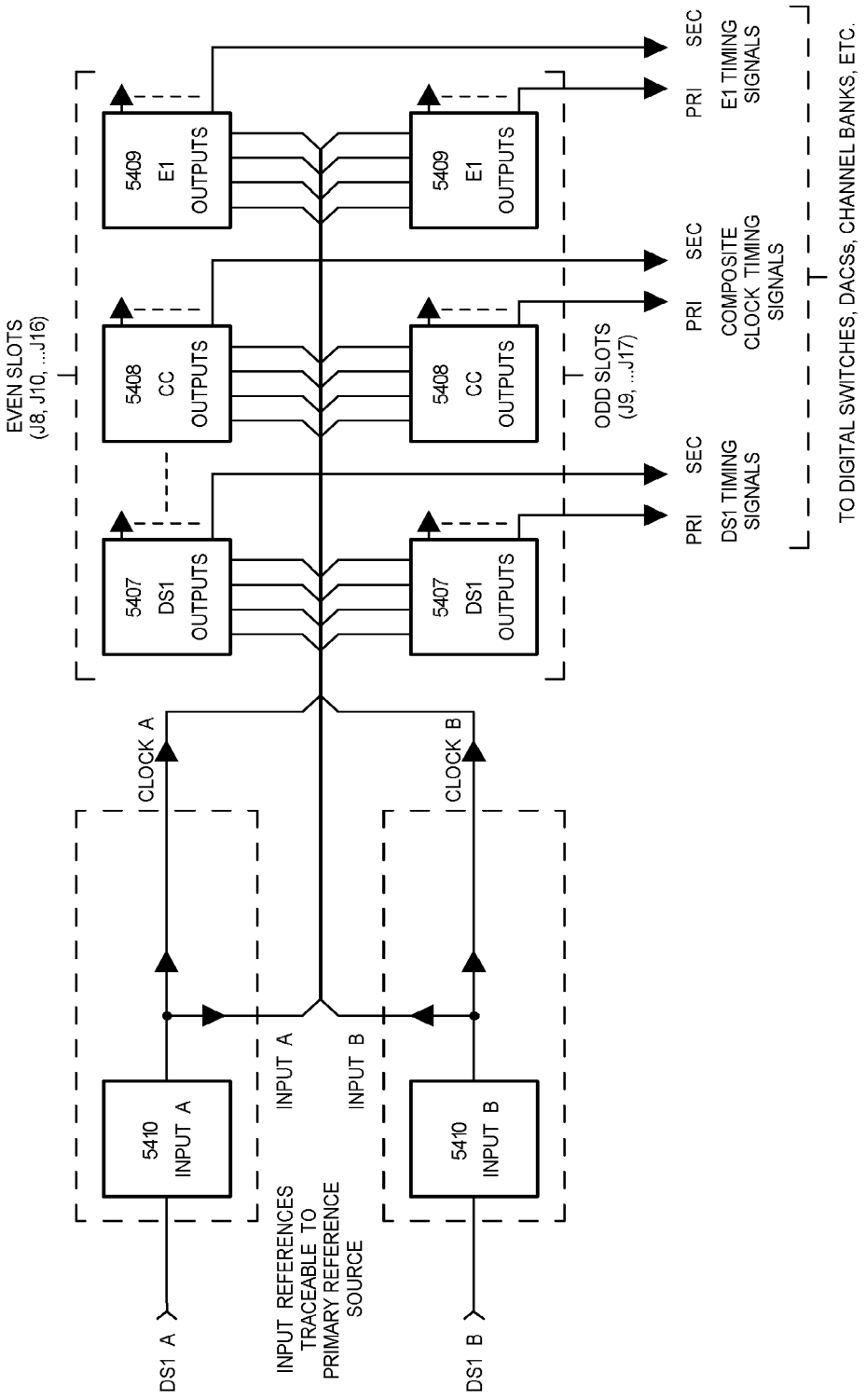


Figure 2-3. Model STS 5400 Stratum 1/2 Application Diagram (5410)

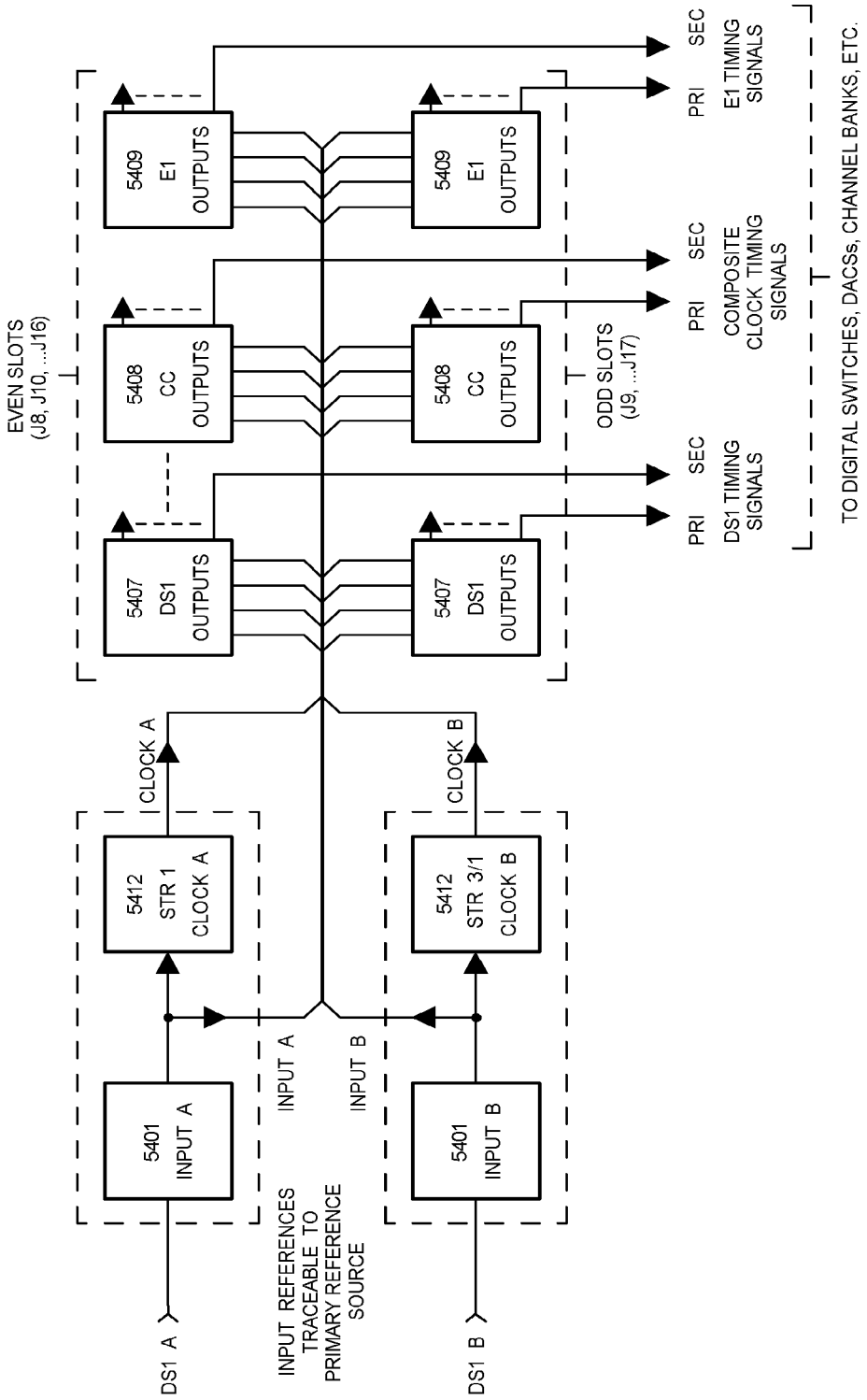


Figure 2-4. Model STS 5400 Stratum 1/3E Application Diagram (5412)

2.212 A synchronization network has two elements, interoffice and intraoffice. The interoffice network consists of primary and secondary DS1 links that carry timing between offices in a hierarchical relationship. Intraoffice timing distribution is based on the concept of a master clock, known in North America as Building Integrated Timing Supply (BITS), which provides timing to all other digital equipment in the office. For the purposes of this section, it will be referred to as the Central Clock. See Figure 2-5 and Table 2-A for clock information.

2.22 Interoffice Distribution

2.221 Timing information is distributed to offices through a hierarchy of levels, starting with a PRS. The general plan for this system of levels is described in References 1 and 2 (paragraph 2.25). Clocks are grouped into four stratum levels, based on their ability to maintain accurate timing if their reference fails (holdover mode). Stratum 1 is the most accurate; it is by definition a stand alone PRS which does not have an external reference. Stratum 4 clocks are the least accurate; they have no holdover requirements and are typically found in DS1 terminal equipment such as D4 channel banks. A given clock must be able to track a reference from a free running clock of the same or higher stratum level. Central Clocks in central offices (COs) are either Stratum 2 or Stratum 3 (Larus Stratum 3E Enhanced), with Stratum 2 being used in larger offices where holdover drift can affect hundreds or thousands of outgoing trunks. Requirements for accuracy and stability of the stratum levels are given in References 1 through 4.

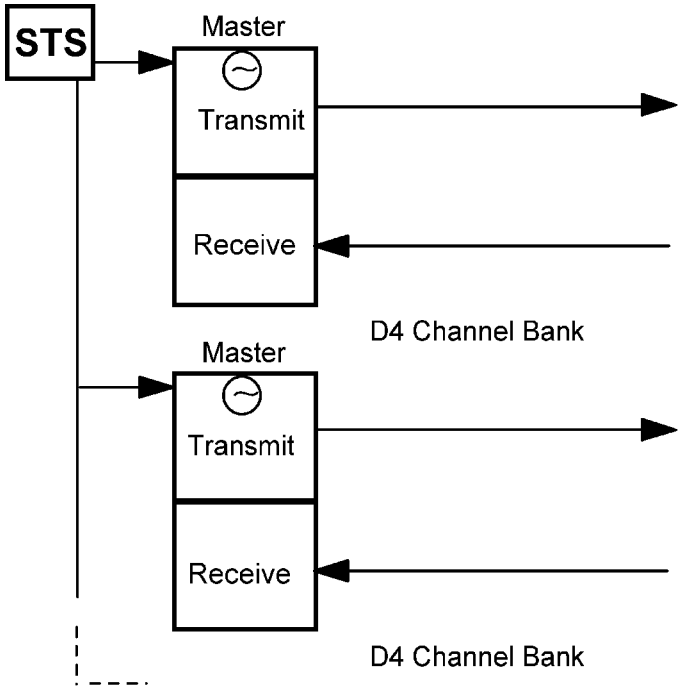
2.222 A synchronization network should be designed so a clock always receives timing from a clock of equal or higher stratum level. It should also ensure that, if an upstream clock enters a hold mode, the downstream clock will be able to track it. Stratum 2 and 3 clocks are provided with primary and secondary timing reference inputs, with automatic switching between the two if either one fails. Timing distribution is typically done with traffic carrying DS1 signals over paths selected for best availability.

2.223 Interface standards for synchronization networks are described in Reference 4.

2.224 The following are the major rules for designing a synchronization network:

a. An office Central Clock can receive its references only from another office or offices of the same or higher stratum level (2 is a higher stratum than 3 and 1 is higher than 2). A higher stratum is preferred, provided reliable diverse DS1 paths from that office exist, but is not required.

(continued)



NOTE: This common reference source is called a Synchronization Timing System (STS). It is intended to feed a reference signal to all digital equipment within a building so that all of the transmission clocks will have a common "heartbeat."

Figure 2-5. Central Clock Concept

Table 2-A

Clock Strata Performance

Stratum	Accuracy, Adjustment Range	Pull-in Range	Stability	Time To First Frame Slip
1	1×10^{-11}	N/A	N/A	72 days
2	1.6×10^{8}	Must be capable of synchronizing to clock with accuracy of $\pm 1.6 \times 10^{-8}$	1×10^{-10}/day	7 days
3E*	4×10^{-7}	4.6×10^{-6}	5×10^{-9}/day	7 hours
3E	1.0×10^{-6}	Must be capable of synchronizing to clock with accuracy of $\pm 4.6 \times 10^{-6}$	1×10^{-8}/day	3.5 hours
3	4.6×10^{-6}	Must be capable of synchronizing to clock with accuracy of $\pm 4.6 \times 10^{-6}$	3.7×10^{-7}/day	6 minutes (255 in 24 hours)
4E	32×10^{-6}	Must be capable of synchronizing to clock with accuracy of $\pm 32 \times 10^{-6}$	Same as accuracy	Not yet specified
4	32×10^{-6}	Must be capable of synchronizing to clock with accuracy of $\pm 32 \times 10^{-6}$	Same as accuracy	N/A

* Larus-enhanced performance. Performance requirements for the remaining stratum levels (except Stratum 3E) are taken from ANSI/T1.101-1994, Synchronization Interface Standard for Telecommunications, and Bellcore GR-1244-CORE, clocks for the Synchronized Network: Common Generic Criteria. The Stratum 3E level is defined only by Bellcore.

2.224 (continued)

b. For a given Central Clock, a DS1 facility with the highest availability should be selected for the primary reference input from an upstream clock. A facility with the next highest availability should be selected for the secondary reference, preferably on a route from a different upstream clock. The availability of a path is determined by its historical failure record, installation or rearrangement activity, facility length and type, protection switching, and the number of repeaters or multiplexers on the path.

c. No timing loops are allowed in the synchronization network for any combination of primary and secondary facilities. The potential for loops exists when either primary or secondary reference signals are passed between clocks of the same stratum. Loops are avoided within an office by distributing timing from the Central Clock in a star network. Detailed rules for avoiding loops in the interoffice network are given in References 1 and 2.

d. There are no fixed rules for the number of Central Clocks that can be used in a cascade. Any clock can track any other clock of equal or higher stratum level and will filter out any jitter and short-term wander introduced along the timing reference path. However, long-term wander (over periods of hours) will accumulate along the cascaded paths from the PRS to a given clock. Depending on the nature and length of the facilities, this may limit the total path length. Furthermore, the failure of a reference path may affect all downstream clocks. For these reasons, the number of cascaded clocks should be minimized as far as possible, consistent with the use of whatever highly reliable reference paths are available in the synchronization network. As an example, it would be preferable to time a Stratum 3 clock from another Stratum 3 clock upstream, which is in turn timed from a Stratum 2 clock through reliable facilities, rather than use a direct path of questionable reliability to that Stratum 2 clock. The objective should always be to maximize the overall availability.

2.23 Intraoffice Distribution

2.231 The Central Clock system, described in Reference 3, is the preferred method of distributing timing within an office. Redundant hardware and automatic switching between primary and secondary reference inputs provide a high degree of availability. The Central Clock supplies timing directly to all digital equipment in the office requiring synchronization, usually by means of DS1 framed ones or a 64 kb composite clock. Many NEs have primary and secondary timing ports; the signals to these should be taken from different output cards of the Central Clock system. The Central Clock may also provide primary and secondary timing signals,

2.231 (continued)

through interoffice synchronization network paths specially selected for high availability, to other Central Clocks in downstream offices.

2.24 SONET

2.241 Special considerations for synchronizing SONET NEs are discussed in References 5 and 6. Although the details are beyond the scope of this document, the most important are these:

a. External timing for SONET NEs from a Central Clock is the preferred mode where Central Clock is available.

b. When Central Clock timing is not available, other SONET timing modes (line, through, or loop) should be chosen in such a way as to avoid timing loops and to minimize the length of timing paths.

c. The use of secondary references should follow the rules in References 1 and 2 to avoid timing loops. If a string of more than one SONET add drop multiplexer (ADM) exists between Central Clock timed offices, no secondary references should be used. This also applies to ring configurations; timing should be passed in one direction only, between line timed ADMs. This guideline applies until synchronization messages, now under discussion in the T1X1 committee, can be implemented.

d. It is recommended that payload DS1s carried on SONET not be used for synchronization distribution. These DS1s are subject to phase transients (pointer adjustments) that do not meet short-term stability requirements.

e. SONET NEs may have the capability of deriving a DS1 timing signal that is not part of the payload but is locked to the incoming OC-N line rate. This signal could be used for synchronization distribution. However, it is recommended that synchronization not be passed in this way along a route that has line or through timed ADMs until synchronization messages are implemented. Otherwise, the downstream NE has no way of knowing whether the intermediate ADM has a receive failure and is running on its internal clock.

2.25 References

1. AT&T Tech Pub 60110, 1983, Digital Synchronization Network Plan.

2. Bellcore TA-NPL-000436, Issue 2, 1993.

3. Bellcore TA-TSY-000378, 1986, Timing Signal Generator Requirements and Objectives.

4. ANSI/T1.101-1994, Synchronization Interface Standards for Digital Networks.

5. Bellcore TR-NWT-000253, 1991, SONET Transport Systems: Common Generic Criteria.

6. Bellcore SR-NWT-002224, 1992, SONET Synchronization Planning Guidelines.

7. Bellcore GR-1244-CORE, May 1995, Clocks for the Synchronized Network: Common Generic Criteria.

Specifications 3

3.1 General

3.101 The electrical, physical, and environmental specifications of the Model STS 5400 system are listed in the following paragraphs.

3.2 Mounting Shelf and Environment

3.21 Model STS 5400 Mounting Shelf

3.211 Shelf Power:
–48 Vdc nominal; current drain (fully loaded):

	Stratum 3E Enhanced	Stratum 2
Cold start	2.28 amps	3.80 amps
After warmup	1.83 amps	2.20 amps

3.212 System Supply Voltage:
–42 Vdc to –57 Vdc

3.213 Approximate Power Consumption (fully loaded):

	Initial (cold)	Steady-state
Stratum 1	187 watts	110 watts (after 15 minutes)
Stratum 2	182 watts	105 watts (after 15 minutes)
Stratum 3E Enhanced	110 watts	88 watts (after 5 minutes)
10 MHz Signal Tracking Card	57 watts	57 watts

3.214 Card Fuses (Type GMT):

5401, 5404, 5405	0.75 amp
All others	2.00 amps

3.22 Environmental Limitations

3.221 Operating Temperature:
0°C to 45°C

The 5402, 5403, 5410, and 5412 track and hold cards operate at any ambient temperature within this range; however, their performance to specification requires two additional temperature restrictions.

The ambient air temperature surrounding the track and hold cards must be controlled to ±5°C with respect to the normal or average ambient temperature. That is, the ambient temperature may reside within 0°C to 45°C, but the variance in temperature must be held to a 5°C deviation for the duration of the measurement in order to guarantee the clock specifications. Additionally, the slew rate of ambient temperature change, within the 5°C deviation limit, must be limited to 8°C per hour.

3.222 Storage Temperature:
–40°C to 70°C

3.223 Humidity:
0 % to 95 %, noncondensing

3.224 Shelf Dimensions:
19.00"W x 12.10"D x 12.25"H

3.225 Weight:
28 lbs maximum per shelf, fully equipped

3.226 Compliance with industry standards:
Meets Bellcore Network Equipment Building System (NEBS) standard TR-NWT-000063, Issue 4, July 1991.

3.3 Cards

3.31 Model 5401 DS1 Bridging Input Card

3.311 For switch location and front panel of the Model 5401, refer to Figure 3-1.

3.312 Input Signals:

Three input alternatives when used in conjunction with the backplane:

a. Terminating input, 100 ohms, digital signal crossconnect (DSX-1) signal per AT&T CB 119 and CCITT G.703. Pulse amplitude range 0.5 volt to 3.6 volts peak.

b. Bridging input, 964 ohms. Same signal levels as item a.

c. Monitor input, 100 ohms. Pulse amplitude range 0.05 volt to 0.36 volt peak. For use with external 432 ohm bridging.

3.313 Framing Format:
Superframe (SF) or extended superframe (ESF) switch selectable

3.314 Line Code:
Alternate mark inversion (AMI) or bipolar eight zero substitution (B8ZS), automatic selection

3.315 Duty Cycle:
50 %

3.316 Mark Density:
Not less than 12.5 %; no more than 15 consecutive zeros

3.317 Input Impedance when used in conjunction with the backplane (input impedance of the card alone is >3.3 K ohms):

a. Input a 100 ohms ±5 %
b. Input b 964 ohms ±5 %
c. Input c 100 ohms ±5 %

3.318 Connector (on backplane):
Three pairs of wirewrap terminals for 22 AWG shielded pair cable

3.319 Jitter Tolerance:
Per Bellcore TR-NWT-000499, Issue 4, April 1992, and CCITT G.824

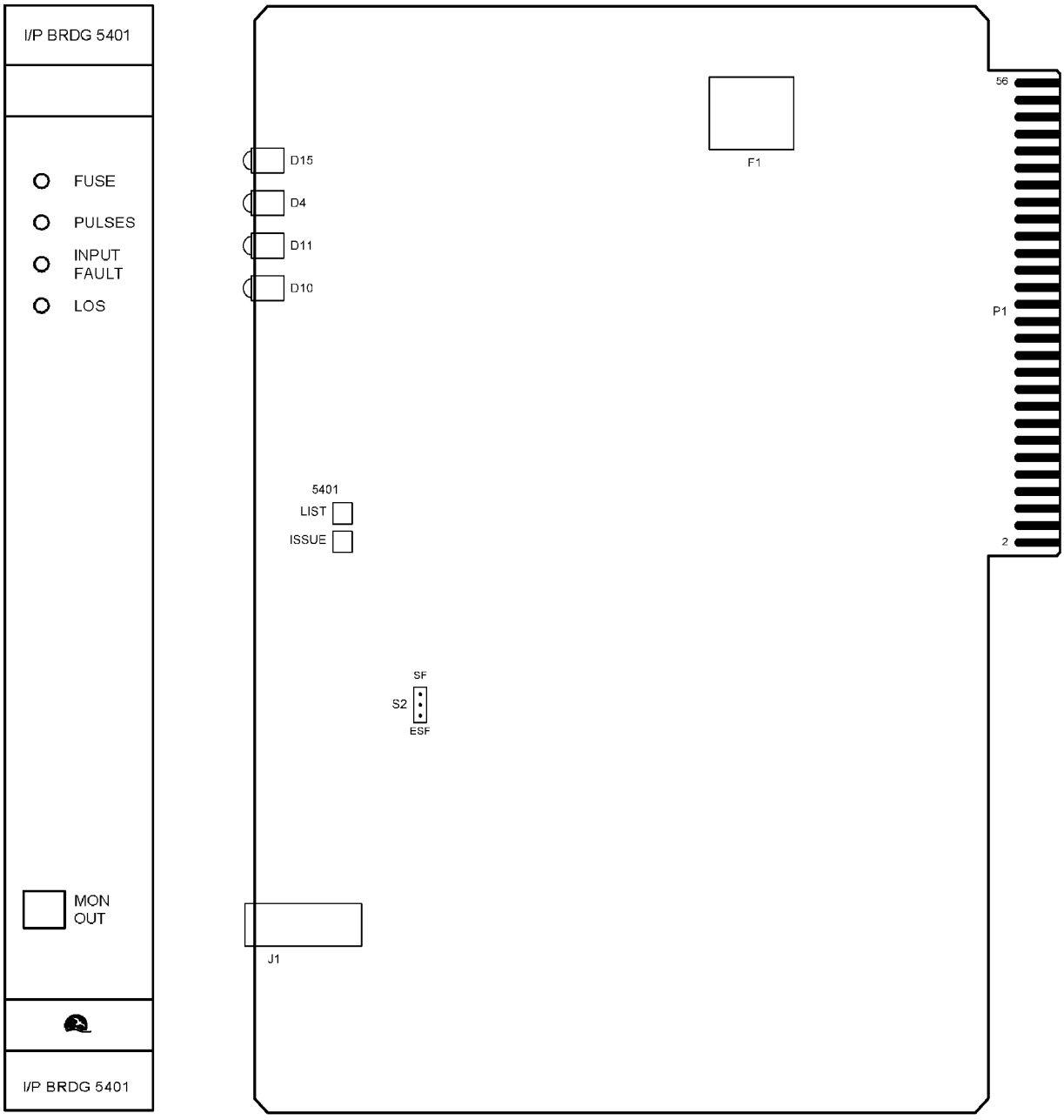


Figure 3-1. Model 5401 DS1 Bridging Input Card with Front Panel

3.3110 Model 5401, Output Signals:

a. 1.544 MHz clock and dual rail data recovered from input, differential outputs on the backplane to both 5402 Track and Hold Cards.

b. Differential recovered input signal to output driver cards (used only if both clock cards fail).

c. Alarm signal to 5406 Alarm Interface Card and 5405 Information Management Card.

d. Front panel Digital Signal Level 1 (DS1) monitor jack (–20 dB) for recovered signal.

3.3111 Light Emitting Diode (LED) Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
PULSES	Green	Input pulses present
INPUT FAULT	Yellow	Input fault [excess Bipolar Violations (BPVs)]
LOS	Red	Loss of signal (LOS) (no clock recovery) or loss of frame (LOF), including the alarm indication signal (AIS)

3.3112 Card Power:
–48 volts, 40 mA

3.3113 Power Fuse:
0.75 amp, Type GMT

3.3114 Fuse Alarm:
Closure to battery

3.32 Model 5402 Stratum 3E Enhanced Track and Hold Card

3.321 For switch locations and front panel of the Model 5402, refer to Figure 3-2.

3.322 Provisioning:

Model 5402-3 supports the AB input architecture.
Model 5402-4 supports the AA input architecture.

NOTE:

A description of the AA versus AB input architecture is provided in Appendix A.

3.323 Input Signals:
Recovered clock and dual rail data from 5401 Input Cards, differential, nominal 1.544 MHz, tracks within ±7.1 Hz

3.324 Framing Format:
Does not apply

3.325 Line Code:
Does not apply

3.326 Input Impedance:
Does not apply

3.327 Jitter Tolerance:
Does not apply

3.328 Input Signal Selection:
Track and Hold Card A input is normally from Input Card A and B input is from Input Card B. If normal input fails, the track and hold card enters the HOLD state and an alarm is posted. Selection of the other input can be performed through the 5405 Information Management Card.

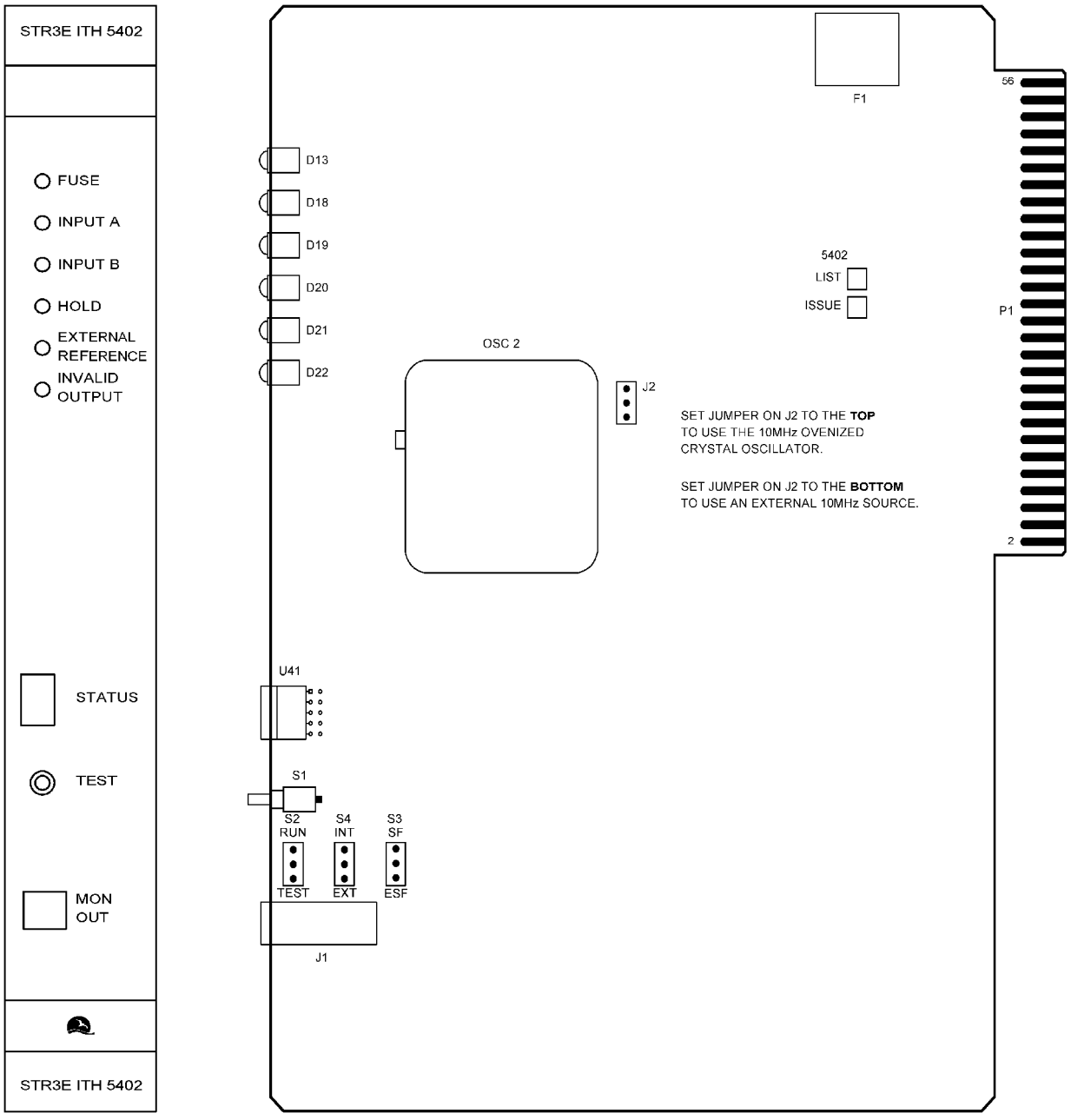


Figure 3-2. Model 5402 Stratum 3E Enhanced Track and Hold Card with Front Panel

3.329 Model 5402, External 10 MHz Reference/Input:
± 1 $volt_{peak}$ square or sine wave into 50 ohm termination. The signal performance characteristics should be equal to or better than those of the track and hold card. This signal may be used in either of the following ways:

a. External Reference:

The signal can be used to replace the on-board 10 MHz oscillator. It is intended that the 10 MHz signal come from an external Global Positioning System (GPS) receiver, cesium oscillator, or similar source. Selection of the external reference is done by on-board jumpers/switches. See Volume 2 of this practice series (Installation) for details.

b. Tracking Input:

The signal can be used as a tracking input. Selection of the 10 MHz tracking input may be done only through the user interface of the 5405 Information Management Card. See Volume 3 (TL1) or Volume 4 (Menu) for command information.

NOTE:

Use of the external 10 MHz signal as both a reference and a tracking input is possible but is not an acceptable mode of operation.

3.3210 Oscillator:
Ovenized crystal oscillator exceeds Stratum 3E specifications.

3.3211 Accuracy (20 years):
1.544 MHz $\pm 4.6 \times 10^{-7}$

3.3212 Pull-in Range (after 96 hours stabilization):
1.544 MHz $\pm 4.6 \times 10^{-6}$ (± 7.1 Hz)

3.3213 Holdover Drift:
$< 5 \times 10^{-9}$ per day over any $\pm 10°C$ temperature range

3.3214 Traceability:
$< 1 \times 10^{-11}$

3.3215 Model 5402, Warmup Time:
Approximately 5 minutes from cold start

NOTE:

The 5407, 5408, 5409, and 5413 output cards will not deliver an output whose frequency is within specification until the 5402 card has completed its warmup cycle following plug-in or power turn-on.

3.3216 Acquisition Time (refer to the clock state diagram, Figure 3-3):

a. From power-up after warmup time:
100 seconds (ACQUIRE 1 state), followed by 300 seconds (ACQUIRE 2 state). Thus, initial entry into normal tracking mode is 12 minutes from cold start (5 minutes plus 400 seconds).

b. From HOLD state returning to normal tracking:
300 seconds (ACQUIRE 2 state).

3.3217 Settling time:
3000 seconds in normal tracking state

3.3218 Output Signals:

a. Ovenized crystal oscillator, derived from nominal clock frequency of 1.544 MHz, tracks input reference or holding; differential backplane signal drives up to ten output cards and 5404 Synchronization Monitor Card.

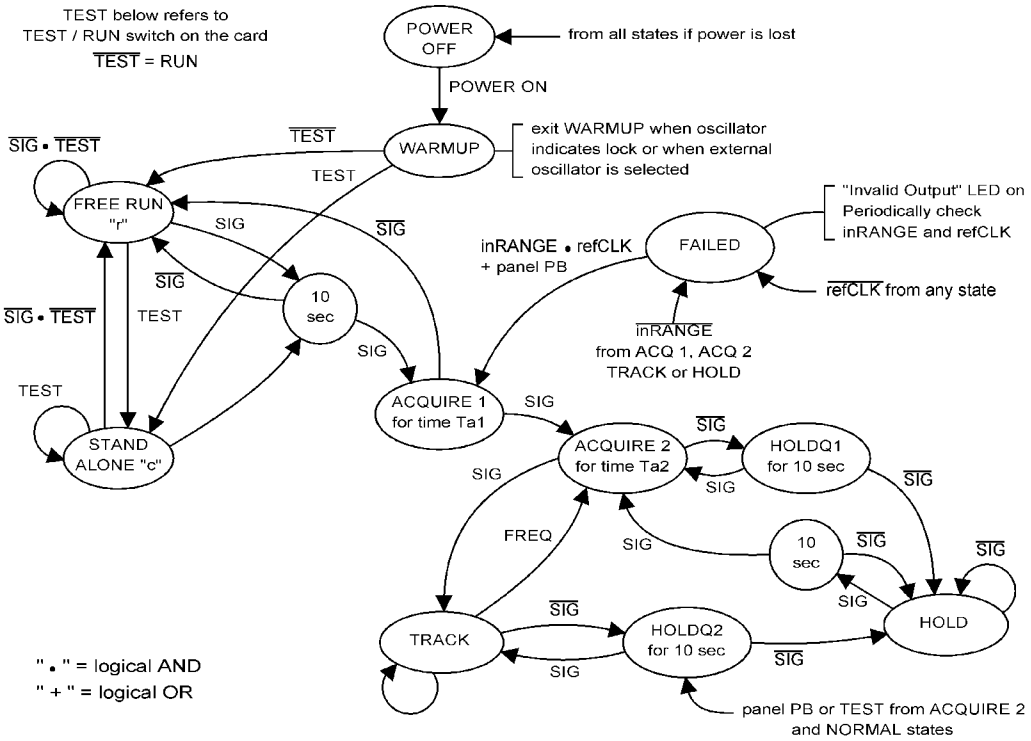
b. DS1 clock monitor, framed all ones.

c. Hold indication bus to output cards.

d. Combined software/hardware alarm indication to 5406 Alarm Interface Card.

e. Hardware alarm indication to 5405 Information Management Card.

f. Serial data link to 5405 Information Management Card for status and control.



Transient states
- ACQUIRE 1, 2 - fast tracking, Ta1 = 100 sec (Stratum 3E), 1200 sec (Stratum 2), Ta2 = 300 sec (Stratum 3E), 1000 sec (Stratum 2)
- HOLDQ1, 2 - hold qualifying states - clock in hold, but not declared
- 10 sec - wait to verify good signal

SIG = CEPT E1 input signal OK
$\overline{SIG}$ = input has LOS or AIS or JITTER or $\frac{\triangle f}{f}$ threshold or OOF
inRANGE = synthesizer control is within tracking range
refCLK = 10 MHz oscillator signal is present (internal or external)
FREQ = frequency difference threshold exceeded (5402E only)

Notes:
1. In both the FREE RUN and STANDALONE states, no tracking has occured since power-up, and the oscillator is set to a predetermined nominal frequency.
2. Operating times per entry:

	Stratum 2	Stratum 3E
ACQUIRE 1	1200 sec	100 sec
ACQUIRE 2	1000 sec	300 sec

3. Approximate settling times:

	Stratum 2	Stratum 3E
ACQUIRE 1	200 sec	70 sec
ACQUIRE 2	1000 sec	225 sec
NORMAL TRACK	9700 sec	3000 sec

The settling times indicated are approximately 3 times the primary (shorter) time constant (except for Stratum 2, Acquire 2, where the indicated settling time is 2.14 times the primary time constant due to the different ratio of the two time constants).
4. This diagram applies to either clock card, for either internal or external 10 MHz references. It does not show clock switching priorities.
5. For discussion of failure of external 10 MHz reference, see Section 5, paragraph 5.4211.

Figure 3-3. Model STS 5400 Clock State Diagram

3.3219 Model 5402, LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
INPUT A	Green	Input A select, tracking
INPUT B	Green	Input B select, tracking
HOLD	Yellow	Hold
EXTERNAL REFERENCE	Yellow	External reference
INVALID OUTPUT	Red	Invalid output

3.3220 Controls and Monitoring:

a. Test pushbutton (press for up to 1 second). In DS1 tracking state, momentary hold test; display shows 'H' if successful. Does not disrupt tracking. In invalid output state, resets tracking algorithm to ACQUIRE 1 state.

b. DS1 monitor jack (–20 dB), SF (D4) or ESF framed all ones at clock output frequency.

3.3221 Seven Segment Status Display:

a. Status conditions while in tracking or acquisition states (display blinks every 1 to 2 seconds):

. ACQUIRE 1 state (single dot).

o At top of display: Normal tracking, no phase error. Alternates with display of input reference.

o At bottom of display: Correction in progress due to more than 1/4 bit phase change.

P Displayed momentarily immediately after power-up.

L Acquiring input reference (warming up).

H HOLD state.

(continued)

3.3221 Model 5402, Seven Segment Status Display (continued)

A Synthesizer control in top 25 % of range.

b Synthesizer control in bottom 25 % of range.

= Primary input in use.

|| Secondary input in use.

c Stand-alone state; switch S1 in TEST position.

r Free running state: No input is present and no tracking has occurred. (Happens on power-up if S1 is in the RUN position and no DS1 input is present.)

b. Error conditions in HOLD state:

2 Excess BPVs; does not cause hold.

3 LOF synchronization.

4 AIS.

5 Input in Yellow Alarm state.

6 Excessive frame bit errors (FBEs); does not cause hold.

7 Outside nominal tracking range of ±7.1 Hz or jitter more than 7 UI peak to peak.

8 Excessive invalid cyclic redundancy check sum (CRC6) codes (for ESF signals only); does not cause hold.

9 LOS (175 consecutive zeros).

c. Error conditions in invalid output state:

O. Overflow | Exit follow mode; unable to phase align.
U. Underflow | Input frequency is too far off.

3.3222 Card Power:
–48 volts, 0.2 amp when cold,
0.15 amp after warmup (5 minutes)

3.3223 Power Fuse:
2 amps, Type GMT

3.3224 Fuse Alarm:
Closure to battery

3.33 Model 5403 Stratum 2 Track and Hold Card

3.331 For switch locations and front panel of the Model 5403, refer to Figure 3-4.

3.332 Provisioning:

Model 5403-3 supports the AB input architecture.
Model 5403-4 supports the AA input architecture.

NOTE:

A description of the AA versus AB input architecture is provided in Appendix A.

3.333 DS1 Input Signals:

Three input alternatives when used in conjunction with the backplane:

a. Terminating input, 100 ohms, DSX-1 signal per AT&T CB 119 and CCITT G.703. Pulse amplitude range 0.5 volt to 3.6 volts peak.

b. Bridging input, 964 ohms. Same signal levels as item a.

c. Monitor input,100 ohms. Pulse amplitude range 0.05 volt to 0.36 volt peak. For use with external 432 ohm bridging.

3.334 Framing Format:
SF or ESF, switch-selectable

3.335 Line Code:
AMI or B8ZS, automatic selection

3.336 Input Impedance when used in conjunction with the backplane (the input impedance of the card alone is >3.3 kohms):

a. Input a 100 ohms ±5 %

b. Input b 964 ohms ±5 %

c. Input c 100 ohms ±5 %

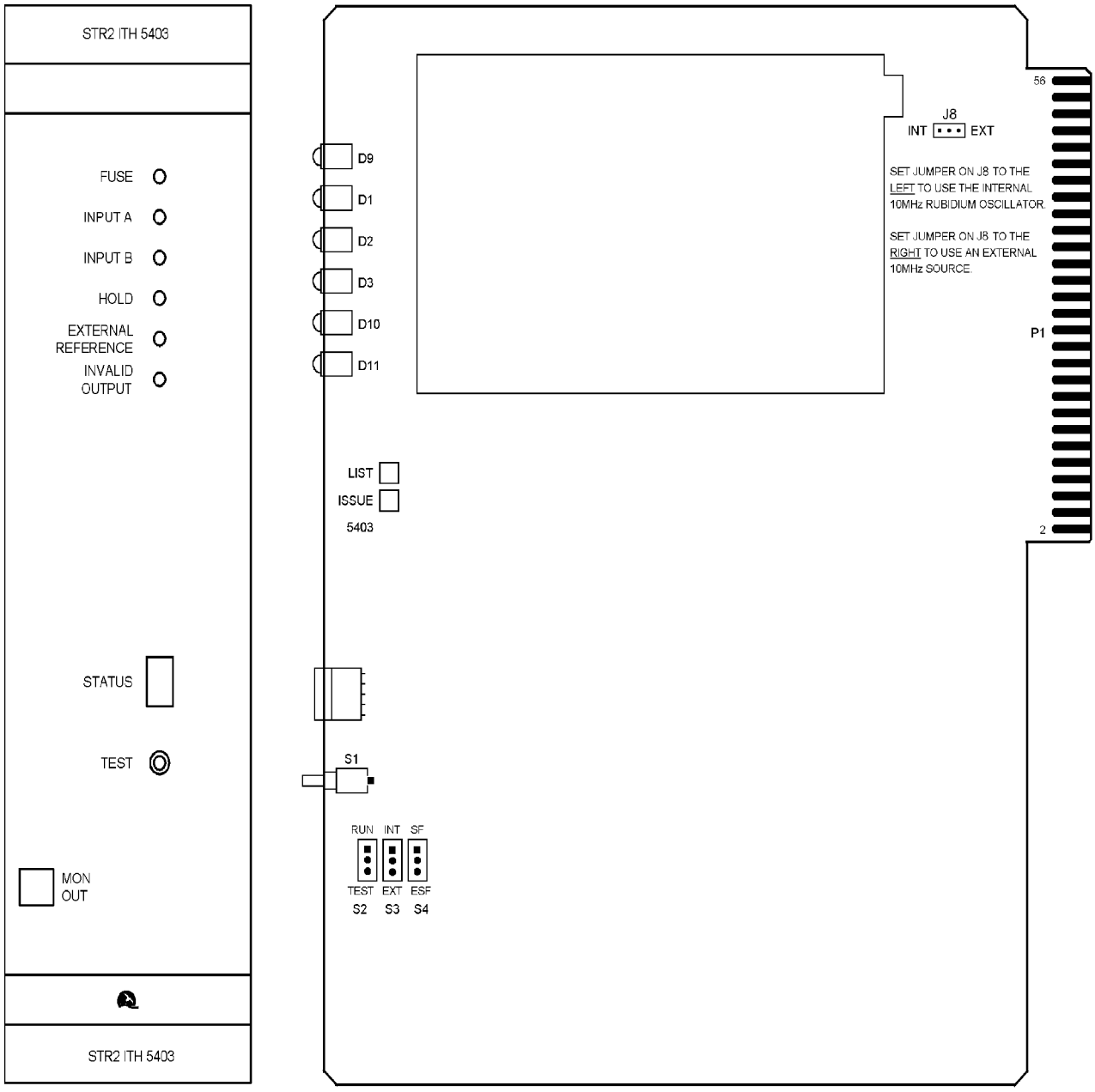


Figure 3-4. Model 5403 Stratum 2 Track and Hold Card with Front Panel

3.337 Model 5403, Jitter Tolerance:
Per Bellcore TR-NWT-000499 and CCITT G.824

3.338 Input Signal Selection:
Track and Hold Card A input is normally from input reference A (primary) and Track and Hold Card B input is from reference B (secondary). If the normal input fails, the clock enters the HOLD state and posts an alarm. Selection of the other input can be performed through the Model 5405 Information Management Card.

3.339 External 10 MHz Reference/Input:
± 1 $volt_{peak}$ square or sine wave into 50 ohm termination. The signal performance characteristics should be equal to or better than those of the track and hold card. This signal may be used in either of the following ways:

a. External Reference:

The signal can be used to replace the on-board 10 MHz oscillator. It is intended that the 10 MHz signal come from an external GPS receiver, cesium oscillator, or similar source. Selection of the external reference is done by on-board jumpers/switches. See Volume 2 (Installation) for details.

b. Tracking Input:

The signal can be used as a tracking input. Selection of the 10 MHz tracking input may only be done through the user interface of the 5405 Information Management Card. See Volume 3 (TL1) or Volume 4 (Menu) for command information.

NOTE:

Use of the external 10 MHz signal as both a reference and a tracking input is possible but is not an acceptable mode of operation.

3.3310 Oscillator:
Rubidium oscillator standard; performance exceeds ANSI* and Bellcore Stratum 2 specifications.

* Registered trademark of the American National Standards Institute, Inc.

3.3311 Long Term Drift (1 year):
1.544 MHz $\pm 5 \times 10^{-10}$ ($\pm 7.72 \times 10^{-4}$ Hz)

3.3312 Model 5403, Pull-in Range:
1.544 MHz $\pm 5 \times 10^{-8}$ ($\pm 7.7 \times 10^{-2}$ Hz)

3.3313 Holdover Drift (after 1 month stabilization):
$< 7.5 \times 10^{-11}$ in one day, over $\pm 5°C$ temperature range.
$< 1 \times 10^{-10}$ after one month, over $\pm 5°C$.

3.3314 Traceability:
$< 1 \times 10^{-11}$

3.3315 Warmup Time:
Approximately 5 minutes from cold start.

NOTE:

The 5407, 5408, 5409, and 5413 output cards will not deliver an output whose frequency is within specification until the 5403 card has completed its warmup cycle following plug-in or power turn-on.

3.3316 Acquisition Times (see Figure 3-3):

a. From power-up, after warmup time:
1200 seconds (ACQUIRE 1 state), followed by 1000 seconds (ACQUIRE 2 state). Thus, normal tracking mode begins 42 minutes after cold start (5 minutes plus 2200 seconds).

b. From HOLD state returning to normal tracking:
1000 seconds (ACQUIRE 2 state).

3.3317 Settling Time:
10,000 seconds in normal tracking state

3.3318 Output Signals:

a. 1.544 MHz rubidium derived clock, tracking input reference or holding; differential backplane signal drives up to ten output cards and a 5404 Synchronization Monitor Card.

b. DS1 clock monitor, framed all ones.

c. Hold indication bus to output cards.

d. Combined software/hardware alarm indication to 5406 Alarm Interface Card.

e. Hardware alarm indication to 5405 Information Management Card.

f. Serial data link to 5405 Information Management Card for status and control.

3.3319 Model 5403, LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
INPUT A	Green	Input A select, tracking
INPUT B	Green	Input B select, tracking
HOLD	Yellow	Hold
EXTERNAL REFERENCE	Yellow	External reference
INVALID OUTPUT	Red	Invalid output

3.3320 Controls and Monitoring:

a. Test pushbutton (press for up to 6 seconds). In the DS1 tracking state, momentary hold test; display shows 'H' if successful. Does not disrupt tracking. In the invalid output state, resets tracking algorithm to ACQUIRE 1 state.

b. DS1 monitor jack (–20 dB), SF (D4) or ESF framed all ones at clock output frequency.

3.3321 Seven Segment Status Display:

a. Tracking or acquisition state status:

. ACQUIRE 1 state (single dot).

o At top of display: Normal tracking;
alternates with display of input reference.

o At bottom of display: Correction in progress due to more than 1/4 bit phase change.

P Power-up cycle; may require up to 5 minutes from a cold start.

L Acquiring input reference (warming up).

(continued)

3.3321 Model 5403, Seven Segment Status Display (continued)

H HOLD mode test successful.

A Synthesizer control in top 25 % of range.

b Synthesizer control in bottom 25 % of range.

= Primary input in use.

|| Secondary input in use.

c Stand-alone state; switch S2 in TEST position.

r Free running mode: No input is present and no tracking has occurred. (Happens on power-up if S2 is in RUN position and there is no DS1 input.)

b. HOLD state error conditions:

2 Excessive BPVs; does not cause hold.

3 LOF synchronization at input.

4 AIS.

5 Input in Yellow Alarm state.

6 Excessive framing bit errors; does not cause hold.

7 Outside nominal tracking range of ±0.04 Hz or jitter more than 7 UI peak to peak.

8 Excessive invalid CRC6 codes (for ESF signals only); does not cause hold.

9 LOS (175 consecutive zeros).

c. Error conditions in invalid output mode:

O. Overflow | Exit follow mode; unable to phase align.
U. Underflow | Input frequency is too far off.

3.3322 Model 5403, Card Power:
–48 volts, 1.2 amp when cold, 0.4 amp after warmup (5 minutes)

3.3323 Power Fuse:
2 amps, Type GMT

3.3324 Fuse Alarm:
Closure to battery

3.34 Model 5404 Synchronization Monitor Card

3.341 For switch locations and front panel of the Model 5404, refer to Figure 3-5.

3.342 The Synchronization Monitor Card is microprocessor-controlled with local or remote selection of alarm thresholds, input to be monitored, observation interval, number of consecutive intervals, and manual or automatic mode. The default mode is an automatic scan with observation interval of 100 seconds per input. Other intervals available are from 1 to 100,000 seconds in decade steps. Inactive inputs are not scanned. Access to this information is through the 5405 Information Management Card.

3.343 Inputs:

a. Five DS1 inputs, SF or ESF framing, AMI or B8ZS line code:

DS1 input reference A (bridges input to clock card A).

DS1 input reference B (bridges input to clock card B).

Three external DS1 inputs: 3, 4, and 5. Input 5 can also be supplied from a front panel jack.

Terminating, bridging, or monitoring input signal. For specifications, refer to paragraphs 3.312 and 3.317.

b. Clock input used as a reference for all phase measurements, transistor-transistor logic (TTL) from clock card A or B, the same clock selected by the output cards of the system, i.e., the better locally available clock.

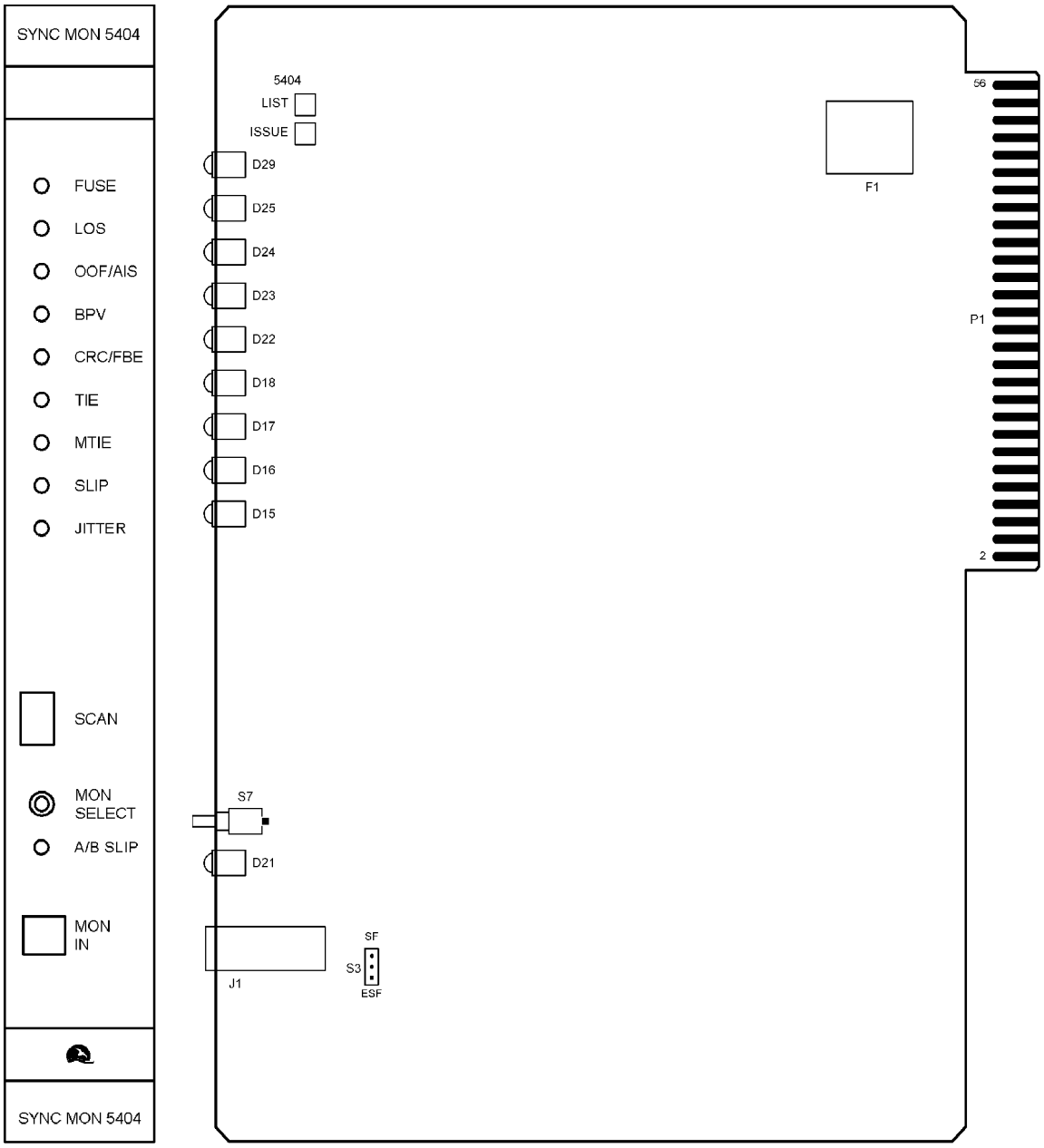


Figure 3-5. Model 5404 Synchronization Monitor Card with Front Panel

3.344 Model 5404, Outputs:

a. Serial data link to 5405 Information Management Card for performance, alarm, and control information.

b. Alarm lead to 5406 Alarm Interface Unit for excess bit slip between clock cards (one bit slip in 30 minutes) or LOF or LOS on input being monitored.

c. Alarm signal to 5405 Information Management Card.

3.345 Measurements:

a. Continuous monitoring of bit slip between clock cards; alarm output to 5405 and 5406 if this is greater than one slip every 30 minutes.

b. DS1 error and performance parameters:

Out of frame (OOF) events (includes AIS)

LOS events

BPV errored seconds count

CRC6 errored seconds counts (for ESF):

Mild – 1 to 319 CRC6 errors
Severe – 320 or more CRC6 errors

Frame errored seconds (for SF)

Timing parameters, using currently active clock as a reference (phase sampling rate about 188 per second):

1. Time interval error (TIE) and maximum time interval error (MTIE) over selected interval.

NOTE:

TIE and MTIE are calculated from phase data processed through a 10 Hz low pass filter.

(continued)

3.345 Model 5404, Measurements (continued)

2. Peak to peak wander below 10 Hz over selected intervals; also over 5-minute or 24-hour intervals.

3. Peak to peak jitter in 10 Hz to 23 kHz band over 1-second intervals.

NOTE:

The clock recovery circuit used for jitter measurement acts as a single pole low pass filter for jitter frequencies above 23 kHz.

3.346 Raw Phase Measurement:
Raw unfiltered phase data for any of the five inputs, 32 phase samples per selectable observation interval, from 1 to 100,000 seconds in decade steps.

3.347 Reporting of Performance Data:
Data are accessed by local or remote terminals through the 5405 Information Management Card in the following modes:

a. Synchronization Monitor Card default (scan) mode:
Continuous scan of active DS1 inputs, accumulating measurements (refer to paragraph 3.345 b.) for 100 seconds for each input. Accumulated values are stored separately for the 24 most recent one-hour intervals on a rotating basis (the last 24 hours are stored at any point). Each complete rollover of 24 one-hour intervals is summarized and stored in totals for each of the past seven days. ESF CRC6 events are broken down into mild errored seconds (at least one but fewer than 320 CRC errors) or severely errored seconds (more than 320 CRC errors). All the stored data can be retrieved on command at any time.

b. Synchronization Monitor Card manual mode:
Remote selection of the parameters to be measured, the inputs to be scanned, the observation interval (1 to 100,000 seconds in decade steps), and the number of consecutive intervals (iterations) to be observed on a given input. Up to 64K iterations can be programmed. Data for the current interval are sent to the terminals at the end of each iteration.

3.347 Model 5404, Reporting of Performance Data (continued)

c. Phase data:
Selection of one of five inputs, the observation interval (1 to 100,000 seconds in decade steps), and the number of consecutive observation intervals to be measured on a given input. Consecutive intervals can be selected, with 32 phase samples per interval.

3.348 Alarm Reporting:

a. Autonomous alarm reports, via the 5405 card, when selected thresholds are exceeded or when the A/B clock slip exceeds one bit in 30 minutes (major alarm).

b. LED indicators, listed below, for thresholds exceeded. Threshold levels are defined in Section 4, Table 4-A.

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
LOS	Yellow	Loss of signal
OOF/AIS	Yellow	Out of frame/alarm indication signal
BPV	Yellow	Bipolar violations rate
CRC/FBE	Yellow	Cyclic redundancy check sum/frame bit errors
TIE	Yellow	Time interval error
MTIE	Yellow	Maximum time interval error
SLIP	Yellow	Slip event (193 bits)
JITTER	Yellow	Jitter
A/B SLIP	Red	A/B clock bit slip

3.349 Seven Segment Status Display:
Briefly shows the new input being monitored when the input is changed; otherwise shows bit slip between the two clock cards.

3.3410 Front Panel Controls (Monitor Select pushbutton):
In the scan mode, a single push advances the 5404 to the next available input.

3.3411 Card Power:
–48 volts, 100 mA

3.3412 Power Fuse:
0.75 amp, Type GMT

3.3413 Fuse Alarm:
Closure to battery

3.35 Model 5405 Information Management Card

3.351 For switch locations and front panel of the Model 5405, refer to Figure 3-6.

3.352 Provisioning:

Model 5405-4 supports the AA input architecture and provides a TL1 interface.

Model 5405-5 supports the AA input architecture and provides a Menu interface.

Model 5405-8 supports the AB input architecture and provides a TL1 interface.

Model 5405-9 supports the AB input architecture and provides a Menu interface.

NOTE:

The Model 5405 version and track and hold card version must support the same input architecture, AA or AB. See Appendix A.

3.353 Inputs:

a. Serial data link from 5404 Synchronization Monitor Card, reporting DS1 performance and timing parameters (refer to paragraph 3.345).

(continued)

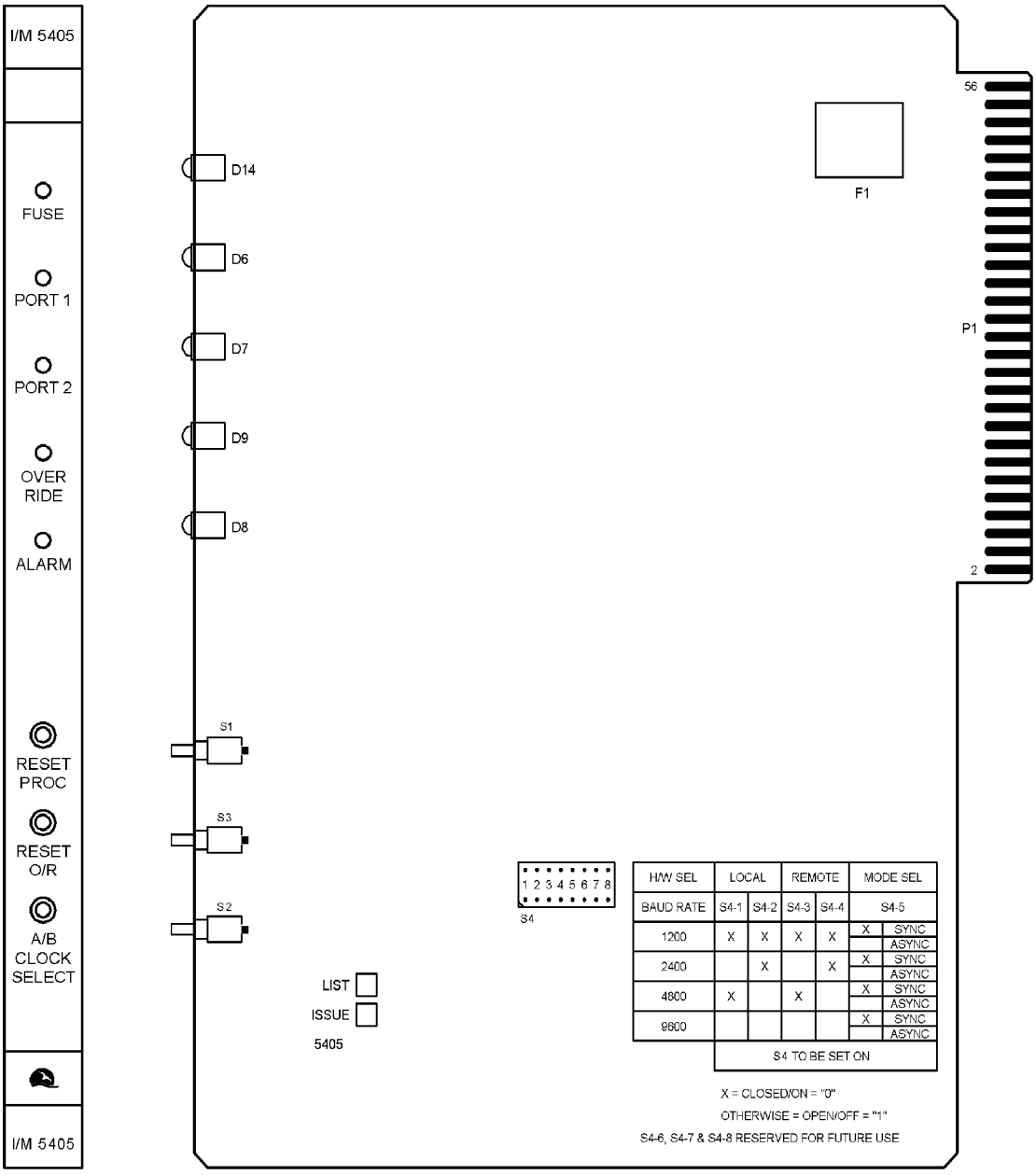


Figure 3-6. Model 5405 Information Management Card with Front Panel

3.353 Model 5405, Inputs (continued)

b. Serial data links from the currently selected 5402, 5403, 5410 or 5412 clock cards reporting their status (tracking, hold, freerun, or failed).

c. Alarm leads from all other cards, including each of the ten output cards.

3.354 Outputs:

a. Serial data link to 5404 Synchronization Monitor Card to set alarm thresholds, measurement intervals, and scanning mode.

b. Serial data links to the currently selected 5402, 5403, 5410, or 5412 clock cards, setting their states (track, hold, etc.).

c. Control lines to output cards, overriding their input selection.

d. Alarm to 5406 Alarm Interface Card.

3.355 Serial Communication Ports:

a. EIA RS-232D for local access by a terminal, providing for information retrieval and control functions in an asynchronous ASCII format with rate selectable from 1200 to 9600 baud. Connection to a terminal requires a crossover cable or null modem.

b. EIA RS-232D for remote access, supporting standard modem control leads. Rates selectable from 1200 to 9600 baud, asynchronous. Modems are connected using 25-wire extension cable.

c. Message format (either of the following):

1. Menu screens Refer to Larus Practice 80-801-193.

2. TL1 language Refer to Larus Practice 80-802-193.

3.356 Model 5405, Serial Port Information (available through Menu or TL1 option):

NOTE:

Three identification (ID) registers, 20 characters each, are remotely settable. These identify the system and the two input reference links. Reports are identified by IDs and are time and date stamped.

a. Status:

Input A or B present/not present.
A and B clock status: tracking, holding, freerun, and control nearing end of the range.
Output card signal selection: CLOCK A, CLOCK B, IN A, or IN B.

b. Alarms (broadcast on occurrence):

Threshold(s) exceeded from Synchronization Monitor Card.
Card alarm, card ID, and major/minor status; refer to paragraph 3.363.

c. Performance:

Alarm events in last 24 hours and in last 7 days.
Synchronization Monitor Card data; refer to paragraph 3.345.

d. Command functions:

Override and select source to output cards.
Set alarm thresholds.
Set scan mode and measurement intervals of the Synchronization Monitor Card.
Set automatic send of performance data.
Set time, date, and ID registers.
Set A or B clock states.
Retrieve Synchronization Monitor Card data.
Retrieve current alarm and status information.
Retrieve alarm log.

NOTE:

This is an abbreviated list. For a complete list, refer to Larus Practice 80-801-193 (Menu) or 80-802-193 (TL1).

3.357 Model 5405, LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
PORT 1	Green	Serial Port 1 active
PORT 2	Green	Serial Port 2 active
OVERRIDE	Yellow	Override active (manual selection of signal to output cards)
ALARM	Red	Alarm

3.358 Front Panel Controls (recessed):

a. Reset processor.

b. Set override.

c. Manual A/B clock select (steps); selects signal to output cards when override is active.

3.359 Card Power:
–48 volts, 100 mA

3.3510 Power Fuse:
0.75 amp, Type GMT

3.3511 Fuse Alarm:
Closure to battery

3.36 Model 5406 Alarm Interface Card

3.361 For card layout and front panel of the Model 5406, refer to Figure 3-7.

3.362 Inputs:
Separate alarm status signals from all cards, including each of the ten output cards.

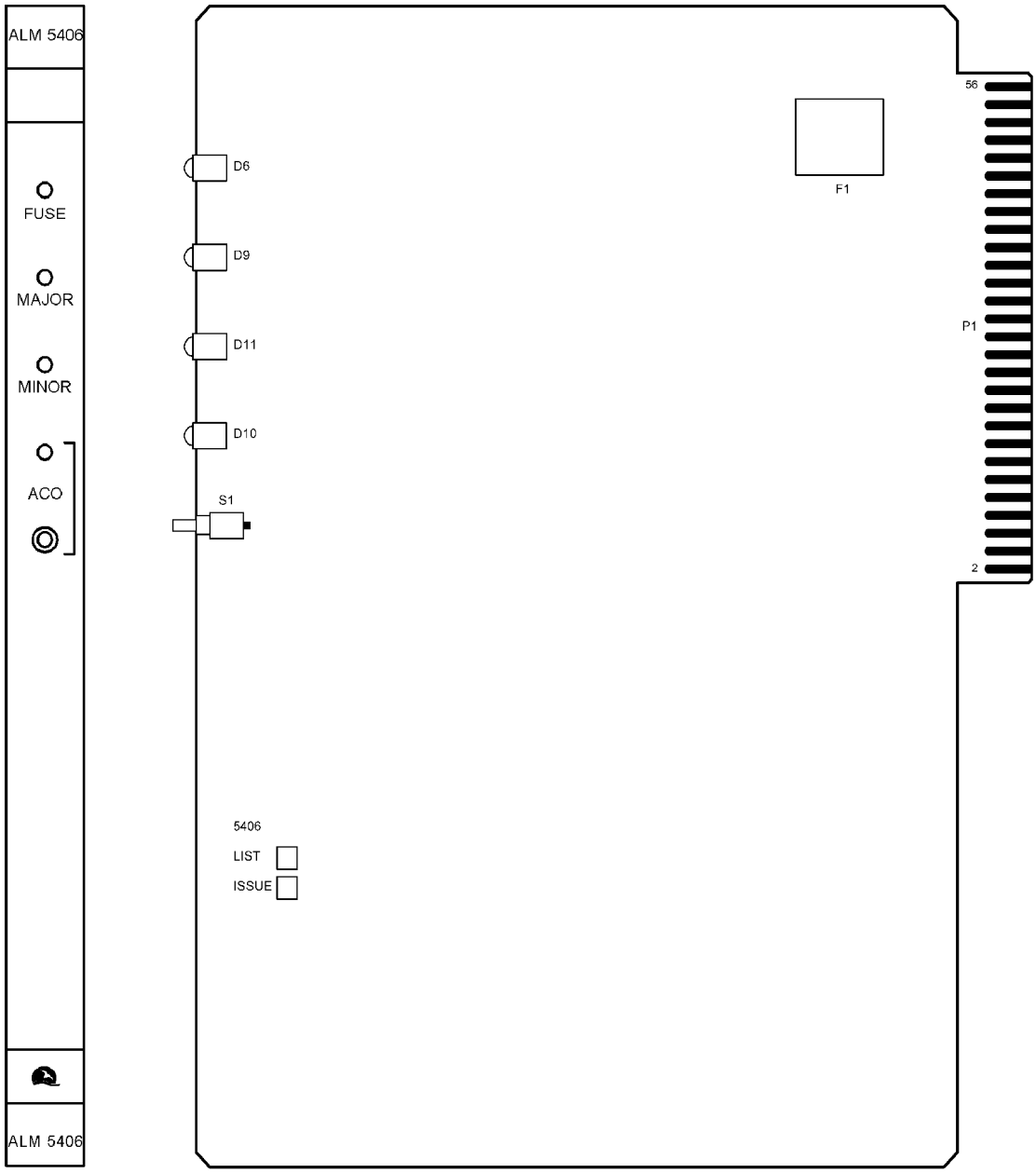


Figure 3-7. Model 5406 Alarm Interface Card with Front Panel

3.363 Model 5406, Outputs:

a. Four floating relay contact closures (form A) for summary major and minor, audible and visual alarms:

Major alarm: Input cards A and B invalid,
OR both Clock A and Clock B not tracking,
OR two or more output cards (even and odd) in alarm,
OR bit slip between A and B Track and Hold Cards reported by the Synchronization Monitor Card.

Minor alarm: Any combination of failures not mentioned above, including the Synchronization Monitor Card and Information Management Card failure alarms.

b. Alarm signal to 5405 Information Management Card.

3.364 Alarm Relay Contact Ratings:

a. Switching power 30 W maximum

b. Switching voltage 220 Vac or 220 Vdc maximum

c. Switching current 1 A maximum

3.365 LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
MAJOR	Red	Major alarm
MINOR	Yellow	Minor alarm
ACO	Yellow	Alarm cutoff

3.366 Controls:
ACO pushbutton; disables audible alarm relays but not front indicators. Automatic reset on next alarm.

3.367 Card Power:
–48 volts, 25 mA

3.368 Model 5406, Power Fuse:
2 amps, Type GMT

3.369 Fuse Alarm:
Closure to battery

3.37 Model 5407 DS1 Output Driver Card

3.371 For switch location and front panel of the Model 5407, refer to Figure 3-8.

3.372 Input Signal:
Differential 1.544 MHz TTL clock signal from one of the two track and hold cards or, if both of these have failed, from one of the two input reference signals. The card provides for automatic selection of these input references. Automatic selection can be overridden by manual remote selection.

3.373 Output Signals:
DS1 framed all ones, SF (D4) or ESF framing, common frame and multiframe synchronization with other DS1 output cards. The leftmost output card produces frame synchronization for the rest of the output cards; plugging in an output card does not cause an error on another card's output.

3.374 Output Load Impedance:
100 ohms, resistive

3.375 Output Pulse Amplitude:
3 volts ±0.3 volt peak; meets AT&T CB 119 and CCITT G.703 requirements

3.376 Duty Cycle:
50 %; pulse interval 648 nanoseconds nominal

3.377 Rearrangement Phase Transient during Switching of Input Signals:
MTIE 324 nanoseconds maximum; phase change rate less than 20 nanoseconds in any 14 milliseconds.

3.378 Number of Outputs:
Ten per card; monitor jack (–20 dB) for output #1

3.379 Output Connectors:
Wirewrap pins for up to 22 AWG shielded pair

3.3710 Drive:
Each output capable of driving a standard DS1 receiver through up to 655 feet of 22 AWG office cable

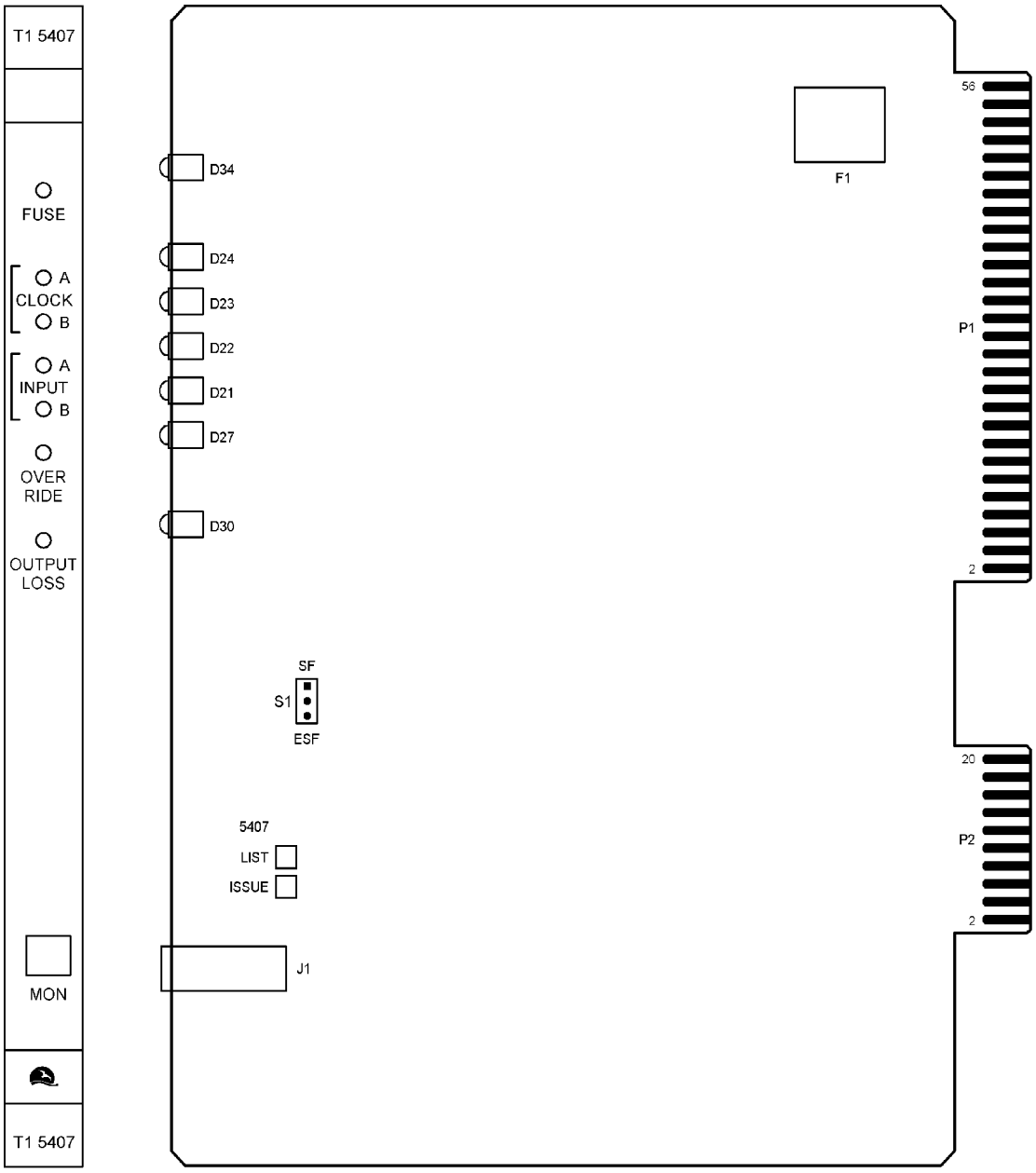


Figure 3-8. Model 5407 DS1 Output Driver Card with Front Panel

3.3711 Model 5407, Output Jitter:
Less than 0.03 UI peak to peak from 10 Hz to 40 kHz

3.3712 Alarms:

a. Alarm line to 5406 Alarm Interface Card; signals loss of one or more outputs.

b. Alarm signal to 5405 Information Management Card.

3.3713 LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
CLOCK A	Green	Clock A selected
CLOCK B	Green	Clock B selected
INPUT A	Yellow	Input A selected
INPUT B	Yellow	Input B selected
OVERRIDE	Yellow	Override (manual selection)
OUTPUT LOSS	Red	Output loss

3.3714 Card Power:
–48 volts, 120 mA

3.3715 Power Fuse:
2 amps, Type GMT

3.3716 Fuse Alarm:
Closure to battery

3.38 Model 5408 Composite Clock Output Driver Card

3.381 For card layout and front panel of the Model 5408, refer to Figure 3-9.

3.382 Input Signal:
Differential 1.544 MHz TTL clock signal from one of the two track and hold cards or, if both of these have failed, from one of the two input reference signals. The card provides for automatic selection of these input references. Automatic selection can be overridden by manual remote selection.

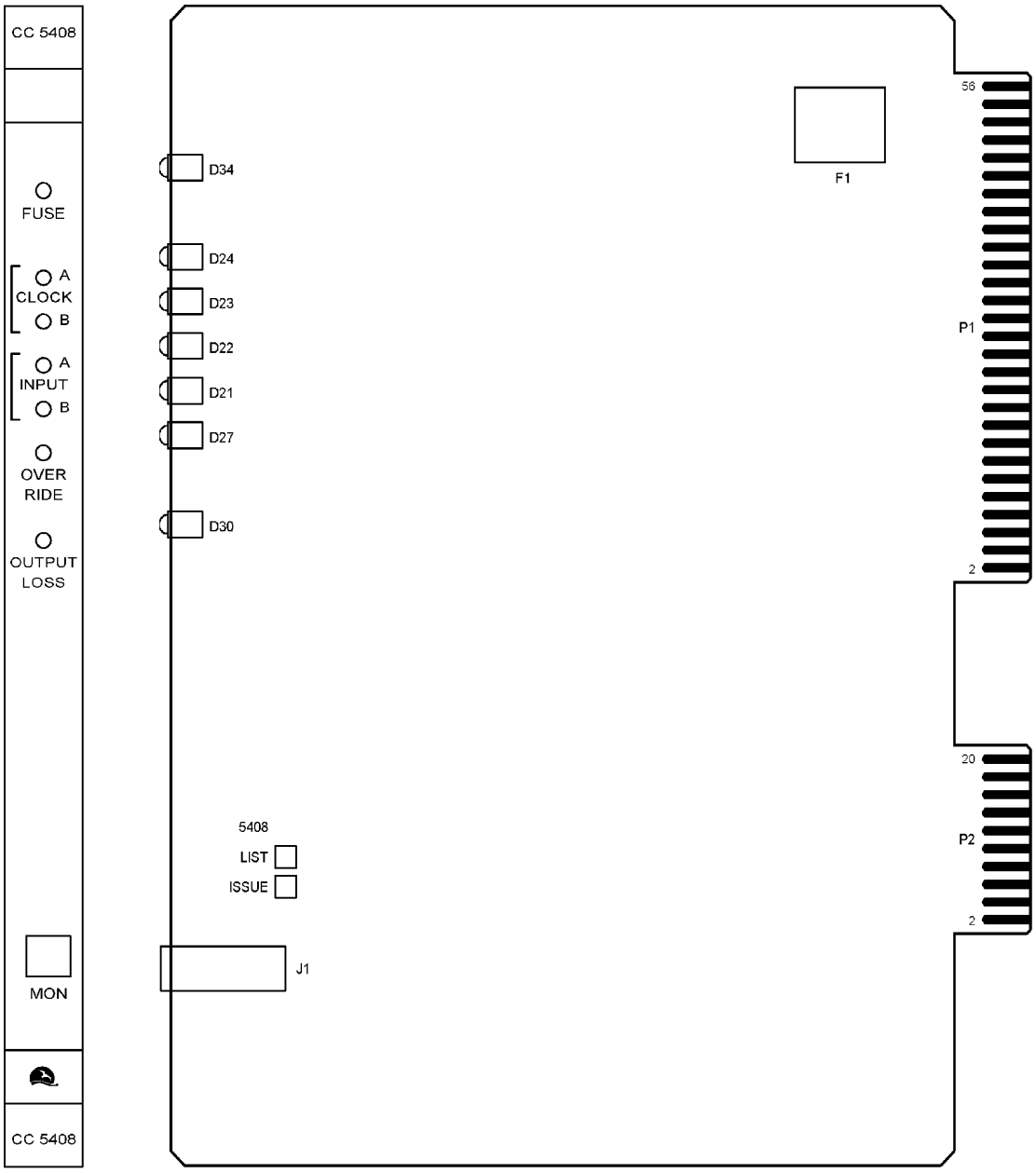


Figure 3-9. Model 5408 Composite Clock Output Driver Card with Front Panel

3.383 Model 5408, Output Signals:

a. 64/8 kbps 5/8 duty cycle pulses.

b. Bipolar pulse violation every eight pulses.

c. Waveshape meeting CCITT G.703.

d. Outputs byte synchronized.

e. Rise time $<$500 nanoseconds.

f. Pulse width 9.765 microseconds $\pm$5 %.

The leftmost output card produces frame synchronization for the rest of the output cards; plugging in an output card does not cause an error on another card's output.

3.384 Output Load Impedance:
133 ohms, resistive

3.385 Output Pulse Amplitude:
3.5 volts $\pm$0.5 volt peak

3.386 Number of Outputs:
Ten per card; monitor jack (–20 dB) for output #1

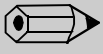
3.387 Connectors:
Wirewrap pins for up to 22 AWG shielded pair

3.388 Drive:
Each output capable of driving up to 1500 feet of 22 AWG office cable

3.389 Alarms:

a. Alarm line to 5406 Alarm Interface Card; signals loss of one or more outputs.

b. Alarm signal to 5405 Information Management Card.



NOTE:

Unused outputs must be terminated in 133 ohms for proper operation of the output alarm.

3.3810 Model 5408, LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
CLOCK A	Green	Clock A selected
CLOCK B	Green	Clock B selected
INPUT A	Yellow	Input A selected
INPUT B	Yellow	Input B selected
OVERRIDE	Yellow	Override (manual selection)
OUTPUT LOSS	Red	Loss of one or more outputs

3.3811 Card Power:
–48 volts, 100 mA

3.3812 Power Fuse:
2 amps, Type GMT

3.3813 Fuse Alarm:
Closure to battery

3.39 Model 5409 E1 Output Driver Card

3.391 For card layout and front panel of the Model 5409, refer to Figure 3-10a (Lists 2 and 3) and Figure 3-10b (List 4).

3.392 Input Signal:
Differential 1.544 MHz TTL clock signal from one of the two track and hold cards or, if both of these have failed, from one of the two input reference signals. The card provides for automatic selection of these input references. Automatic selection can be overridden by manual remote selection.

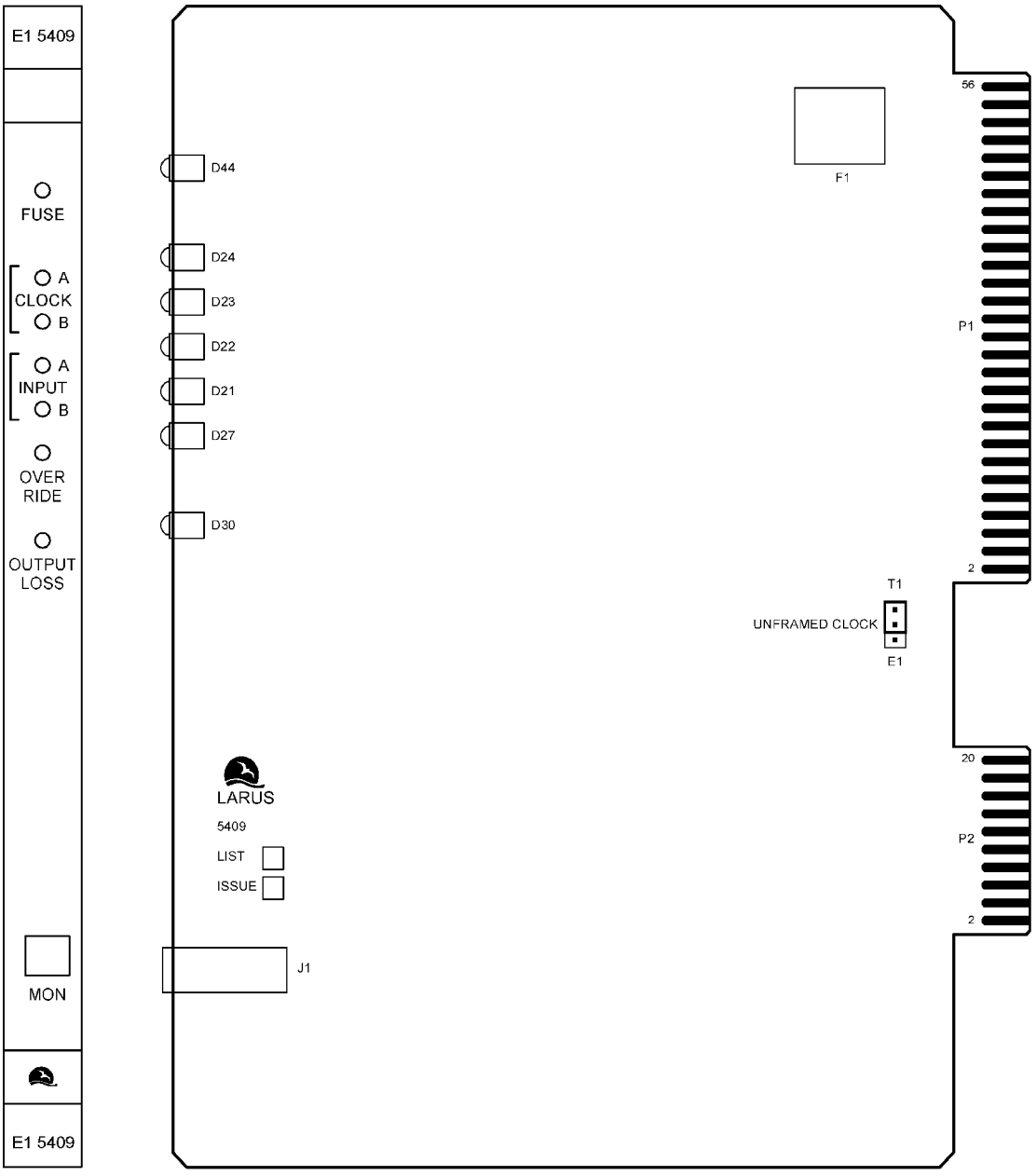


Figure 3-10a. Model 5409-2/-3 E1 Output Driver Card with Front Panel

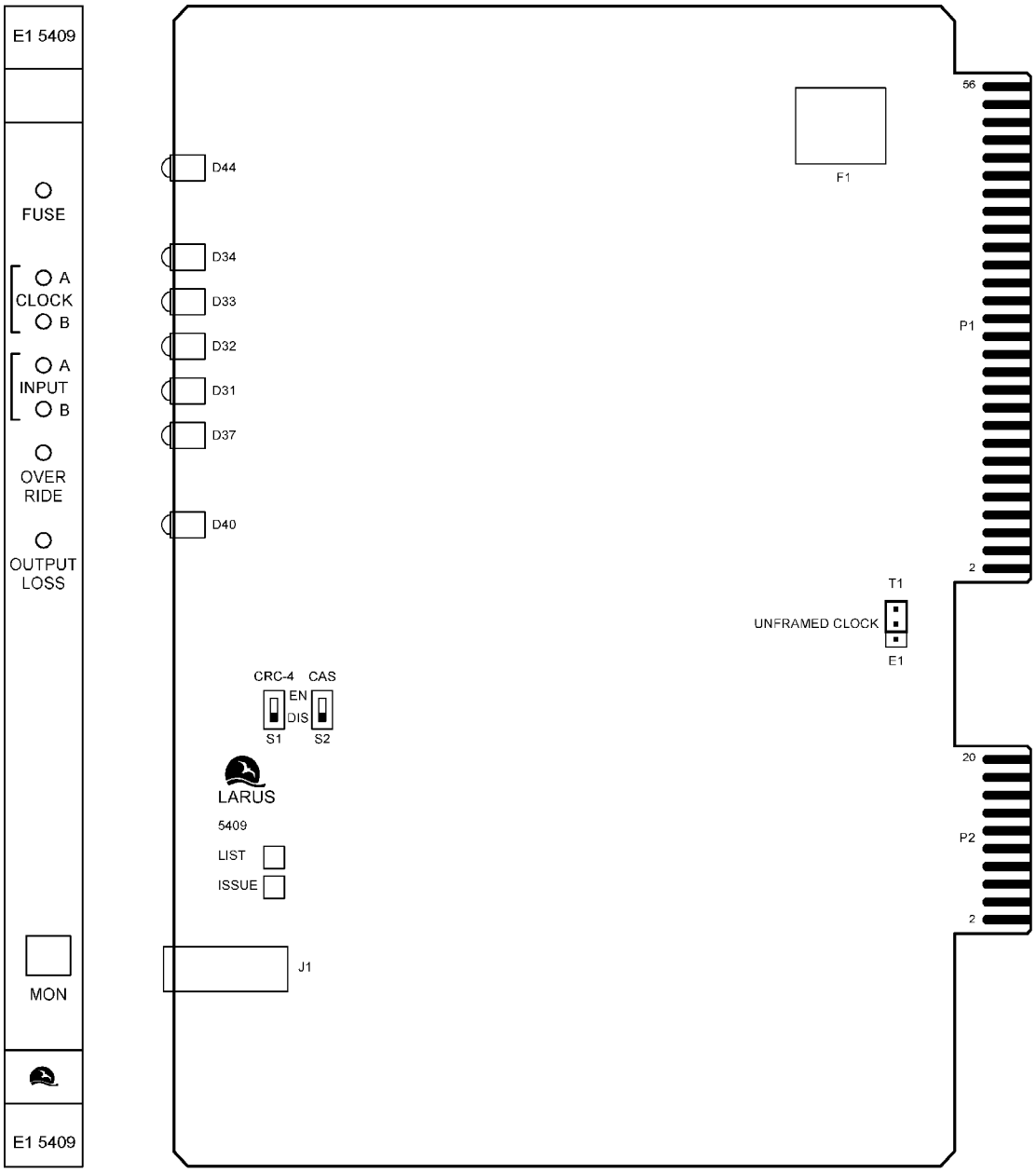


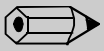
Figure 3-10b. Model 5409-4 E1 Output Driver Card with Front Panel

3.393 Model 5409, Output Signals:

List 2: Bipolar E1 framed all ones, at nominally 2.048 MHz, synchronized to the input at a ratio of 2.048/1.544 = 256/193. Common frame and synchronization with other E1 output cards. CAS and CRC4 multiframe synchronization disabled.

List 3: 2.048 MHz square wave.

List 4: Same as List 2 with addition of configuration switches to enable or disable CAS and CRC4 multiframe synchronization independently.



NOTE:

In a CEPT environment, the data stream always contains the Frame Alignment Signal (FAS) and may contain either one or both of the two kinds of multiframe, namely Cyclic Redundancy Check (CRC4) and Channel Associated Signaling (CAS).

The 5409-4 card allows the user, depending on the system application, to enable or disable either of the two types of multiframe. Refer to Figure 3-10b.

The leftmost output card produces frame synchronization for the rest of the output cards; plugging in an output card does not cause an error on another card's output.

3.394 Output Load Impedance:
120 ohms, resistive

3.395 Output Pulse Format (refer to CCITT G.703 Standard):

List 2,
List 4: Bipolar E1 framed all ones, 3 volts ±0.3 volt peak. Meets Table 6/G.703 and Figure 15/G.703 of the above standard.

List 3: 2.048 MHz square wave, 1.0 to 1.9 volt peak. Meets Table 10/G.703 and Figure 21/G.703 of the above standard.

3.396 Number of Outputs:
Ten per card; monitor jack (–20 dB) for output #1

3.397 Output Connectors:
Wirewrap pins for up to 22 AWG shielded cable

3.398 Output Jitter:
Less than 0.03 UI peak to peak from 20 Hz to 100 kHz

3.399 Drive:
Each output capable of driving a 120 ohm load through up to 200 meters of 22 AWG cable

3.3910 Alarms:

a. Alarm line to 5406 Alarm Interface Card signals loss of one or more outputs.

b. Alarm signal to 5405 Information Management Card.

3.3911 LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
CLOCK A	Green	Clock A selected
CLOCK B	Green	Clock B selected
INPUT A	Yellow	Input A selected
INPUT B	Yellow	Input B selected
OVERRIDE	Yellow	Override (manual selection)
OUTPUT LOSS	Red	Output loss

3.3912 Card Power:
–48 volts, 100 mA

3.3913 Power Fuse:
2 amps, Type GMT

3.3914 Fuse Alarm:
Closure to battery

3.310 Model 5410 GPS Stratum 1 Track and Stratum 2 Hold Card

3.3101 For switch locations and front panel of the Model 5410, refer to Figure 3-11.

3.3102 This card provides Stratum 1 performance when in GPS mode and backup Stratum 2 performance in the event of a GPS failure.

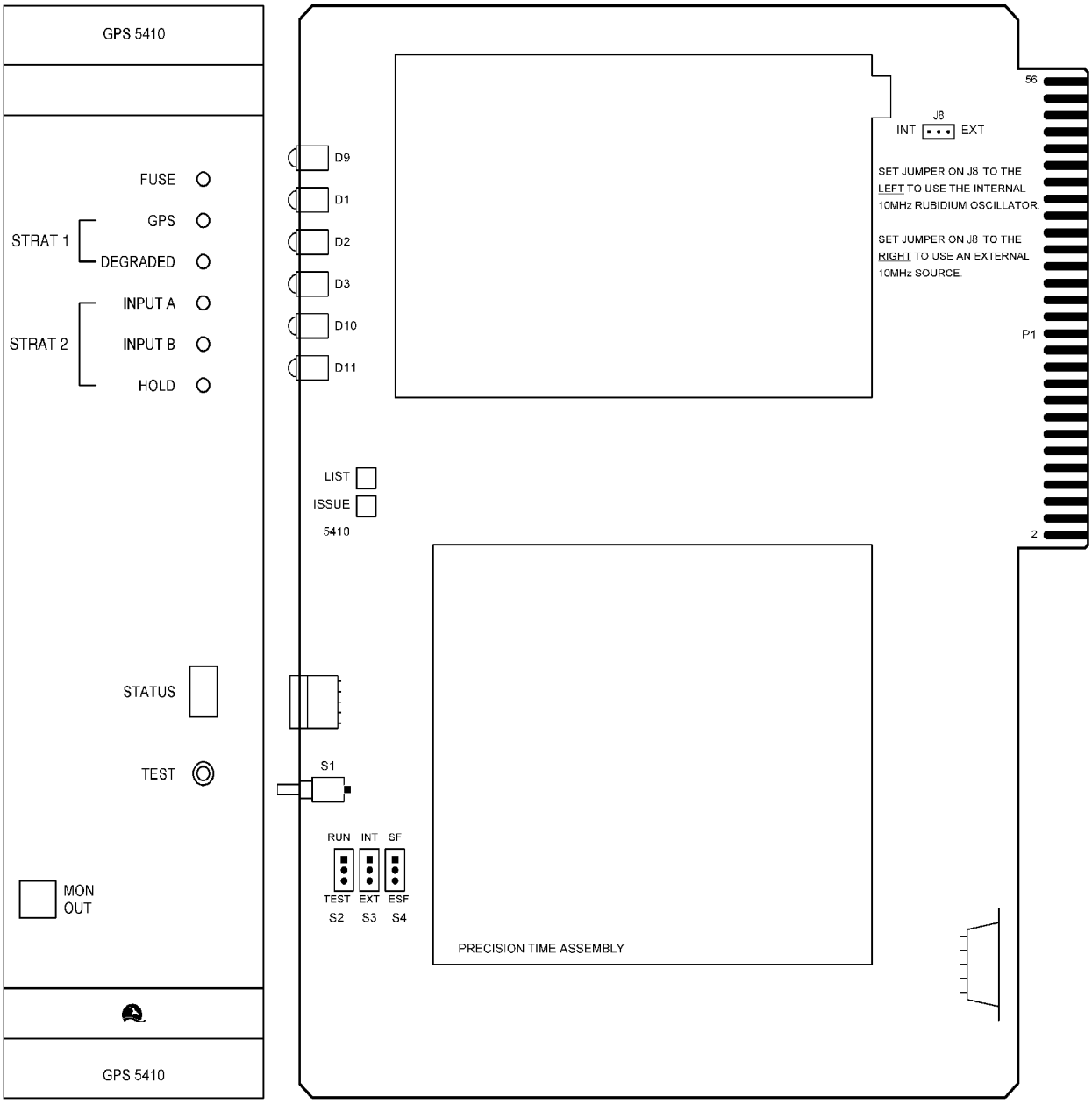


Figure 3-11. Model 5410 GPS Stratum 1 Track and Stratum 2 Hold Card with Front Panel

3.3103 Provisioning:

Model 5410-2 supports the AB input architecture.
The AA input architecture is not supported.

NOTE:

A description of the AB input architecture is provided in Appendix A.

3.3104 Input Signals:

Stratum 1 Primary Reference Source (PRS) is an integral Global Positioning System (GPS) receiver, per Bellcore GR-2830-CORE.

Three secondary input alternatives when used in conjunction with the backplane:

a. Terminating input, 100 ohms, DSX-1 signal per AT&T CB 119 and CCITT G.703. Pulse amplitude range 0.5 V to 3.6 V peak.

b. Bridging input, 964 ohms. Same signal levels as item a.

c. Monitor input, 100 ohms. Pulse amplitude range 0.05 V to 0.36 V peak. For use with external 432 ohm bridging.

3.3105 Framing Format:
SF or ESF, switch-selectable

3.3106 Line Code:
AMI or B8ZS, automatic selection

3.3107 Input Impedance when used in conjunction with the backplane (the input impedance of the card alone is >3.3 kohms):

a. Input a 100 ohms ±5 %

b. Input b 964 ohms ±5 %

c. Input c 100 ohms ±5 %

3.3108 Jitter Tolerance:
Per Bellcore TR-NWT-000499 and CCITT G.824

3.3109 Input Signal Selection:
Clock card A and B inputs are normally from their own fully integrated GPS receiver. If the normal GPS input fails, the clock card will post an alarm and try to acquire the DS1 primary inputs from the backplane. If the DS1 inputs are not present, the clock card will enter the HOLD state and post an alarm.

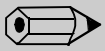
3.31010 Model 5410, External 10 MHz Reference/Input:
± 1 $volt_{peak}$ square or sine wave into 50 ohm termination. The signal performance characteristics should be equal to or better than those of the track and hold card. This signal may be used in either of the following ways:

a. External Reference:

The signal can be used to replace the on-board 10 MHz oscillator. It is intended that the 10 MHz signal come from an external GPS receiver, cesium oscillator, or similar source. Selection of the external reference is done by on-board jumpers/switches. See Volume 2 of this practice series (Installation) for details.

b. Tracking Input:

The signal can be used as a tracking input. Selection of the 10 MHz tracking input may only be done through the user interface of the 5405 Information Management Card. See Volume 3 (TL1) or Volume 4 (Menu) for command information.



NOTE:

Use of the external 10 MHz signal as both a reference and a tracking input is possible but is not an acceptable mode of operation.

3.31011 Oscillator:
Rubidium oscillator standard; performance exceeds ANSI and Bellcore Stratum 2 specifications.

3.31012 Accuracy (20 years):

a. 1.544 MHz $\pm < 1 \times 10^{-11}$ ($\pm < 1.544 \times 10^{-5}$ Hz)
in GPS mode (Stratum 1)

b. 1.544 MHz $\pm 1.6 \times 10^{-9}$ ($\pm 2.5 \times 10^{-3}$ Hz)
if tracking DS1 inputs (Stratum 2)

3.31013 Pull-in Range:

a. 1.544 MHz $\pm < 1 \times 10^{-11}$ ($\pm < 1.544 \times 10^{-5}$ Hz) in GPS mode (Stratum 1)

b. 1.544 MHz $\pm 2.5 \times 10^{-8}$ ($\pm 3.9 \times 10^{-2}$ Hz) if tracking DS1 inputs (Stratum 2)

3.31014 Model 5410, Holdover Drift (after 1 month stabilization):

a. $< 7.5 \times 10^{-11}$ in one day, over $\pm 5°C$ temperature range

b. $< 1 \times 10^{-10}$ after one month, over $\pm 5°C$

3.31015 Traceability:
$< 1 \times 10^{-11}$

3.31016 Warmup Time:
If the 5410 has been unplugged for more than 20 minutes, it can take up to 5 hours before the GPS receiver has achieved Stratum 1 accuracy. If the 5410 has been unplugged for less than 20 minutes, it can take up to 2 hours before the GPS receiver has achieved Stratum 1 accuracy. During this time, the 5410 will be tracking an input signal with Stratum 2 accuracy if a DS1 input signal is present.

NOTE:

The 5407, 5408, 5409, and 5413 output cards will not deliver an output whose frequency is within specification until the 5410 card has completed its warmup cycle following plug-in or power turn-on.

3.31017 Acquisition Times:

a. GPS mode:

1. From power-up after more than 20 minutes off, 5 hours maximum.

2. From power-up after less than 20 minutes off, 2 hours maximum.

b. DS1 mode:

1. From power-up, after warmup time:
1200 seconds (ACQUIRE 1 state).

2. From HOLD state returning to normal tracking:
1000 seconds (ACQUIRE 2 state).

3.31018 Settling Time in DS1 Mode:
10,000 seconds in normal tracking state

3.31019 Output Signals:

a. 1.544 MHz rubidium-derived clock, tracking input reference or holding; differential backplane signal drives up to ten output cards and 5404 Synchronization Monitor Card.

3.31019 (continued)

b. DS1 clock monitor framed all ones.

c. Hold indication bus to output cards.

d. Combined software/hardware alarm indication to 5406 Alarm Interface Card.

e. Hardware alarm indication to 5405 Information Management Card.

f. Serial data link to 5405 Information Management Card for status and control.

3.31020 LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
GPS	Green	Global Positioning System, tracking GPS signal
DEGRADED	Yellow	Degraded, tracking in Stratum 1 Yellow degraded region
INPUT A	Green	Input A select, tracking
INPUT B	Green	Input B select, tracking
HOLD	Yellow	Hold
INPUT A plus INPUT B plus HOLD	Green Green Yellow	Invalid output if all three are illuminated simultaneously

3.31021 Controls and Monitoring:

a. Test pushbutton only valid when tracking DS1 inputs (press for up to 6 seconds). In tracking state, momentary hold test; display shows 'H' if successful. Does not disrupt tracking. In invalid output state, resets tracking algorithm to ACQUIRE 1 state.

b. DS1 monitor jack (–20 dB), SF (D4) or ESF framed all ones at clock output frequency.

3.31022 Seven Segment Status Display:

a. Tracking or acquisition state status:

1 ACQUIRE 1 state.

. External reference (single dot).

o At top of display: Normal tracking; alternates with display of input reference.*

o At bottom of display: Correction in progress due to more than 1/4 bit phase change.*

P Power-up cycle; may require up to 5 minutes from a cold start.

L Acquiring input reference (warming up).

H HOLD mode test successful.*

A Synthesizer control in top 25 % of range.

b Synthesizer control in bottom 25 % of range.

= Primary input in use.*

|| Secondary input in use.*

c Stand-alone state; switch S2 in TEST position.*

r Free running mode: No input is present and no tracking has occurred. (Happens on power-up if S2 is in RUN position and there is no DS1 input.)

b. HOLD state error conditions*:

2 Excessive BPVs; does not cause HOLD.

3 LOF synchronization at input.

4 AIS.

5 Input in Yellow Alarm state.

6 Excessive framing bit errors (FBEs); does not cause hold.

* Only if tracking DS1 reference inputs. Not used in GPS mode.

7 Outside nominal tracking range of ±0.04 Hz or jitter more than 7 UI peak to peak.

8 Excessive invalid CRC6 codes (for ESF signals only); does not cause hold.

9 Loss of input (LOS) (175 consecutive zeros).

c. Error conditions in Invalid Output mode:

O.	Overflow	Exit follow mode; unable to phase align.
U.	Underflow	Input frequency is too far off.

3.31023 Card Power:
–48 volts, 1.2 amp when cold, 0.4 amp after warmup (5 minutes)

3.31024 Power Fuse:
2 amps, Type GMT

3.31025 Fuse Alarm:
Closure to battery

3.311 Model 5412 GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card

3.3111 For card layout and front panel of the Model 5412, refer to Figure 3-12.

3.3112 This is the same as the Model 5402 with the Model 5410's GPS receiver. It provides Stratum 1 performance when in GPS mode and backup Stratum 3E Enhanced performance in the event of a GPS failure.

3.3113 Provisioning:

Model 5412-2 supports the AB input architecture.
The AA input architecture is not supported.

3.3113

NOTE:

A description of the AB input architecture is provided in Appendix A.

3.3114 LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
GPS	Green	Global Positioning System, tracking GPS signal
DEGRADED	Yellow	Degraded, tracking in Stratum 1 Yellow degraded region
INPUT A	Green	Input A select, tracking
INPUT B	Green	Input B select, tracking
HOLD	Yellow	Hold
INPUT A plus INPUT B plus HOLD	Green Green Yellow	Invalid output if all three are illuminated simultaneously

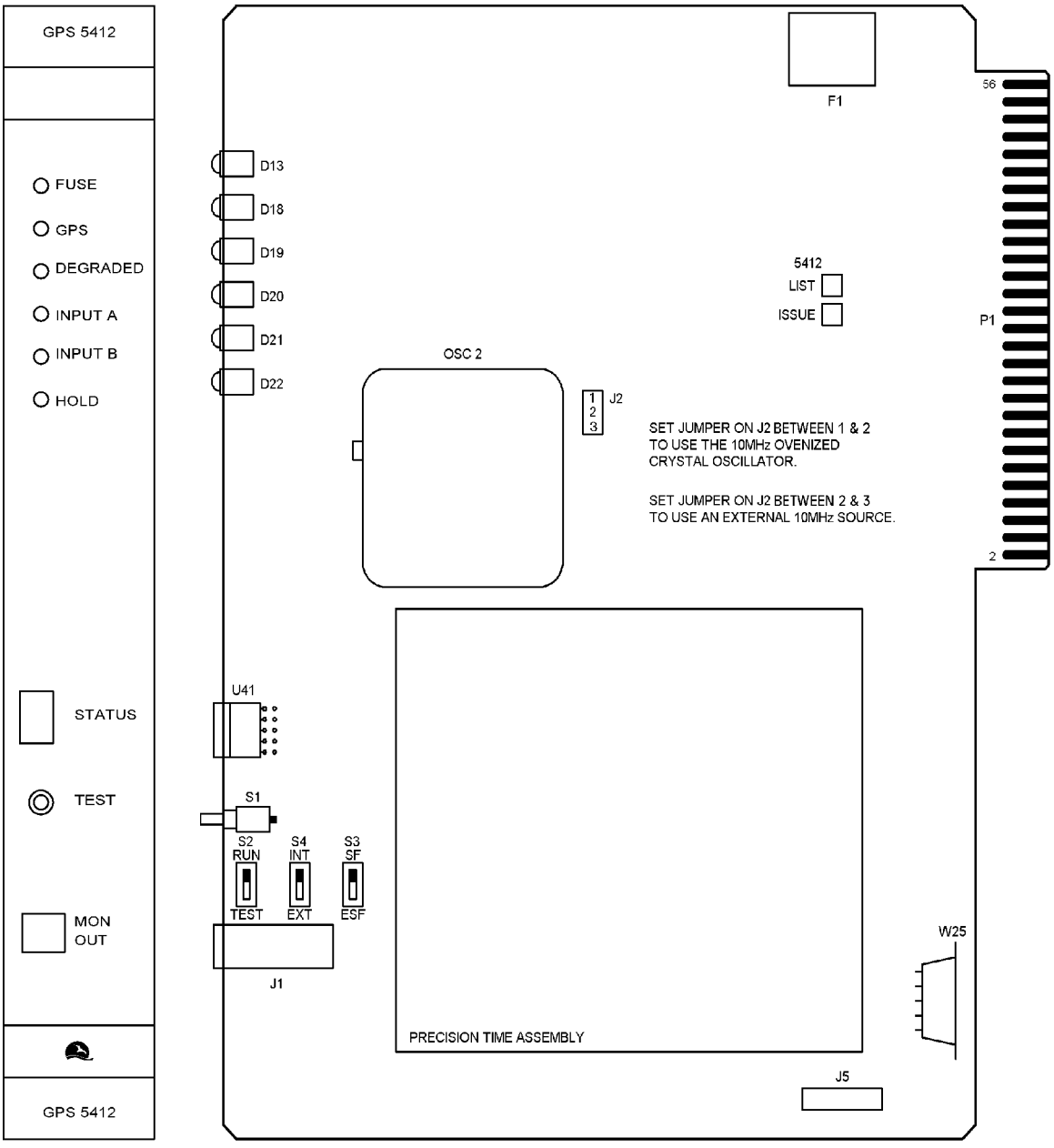


Figure 3-12. Model 5412 GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card with Front Panel

3.3115 Model 5412, Seven Segment Status Display:

a. Status conditions while in tracking or acquisition states; display blinks every 1 to 2 seconds:

1 ACQUIRE 1 state.

. External reference (single dot).

o At top of display: Normal tracking, no phase error. Alternates with display of input reference.

o At bottom of display: Correction in progress due to more than 1/4 bit phase change.

P Displayed momentarily immediately after power-up.

L Acquiring input reference (warming up).

H HOLD state.

A Synthesizer control in top 25 % of range.

b Synthesizer control in bottom 25% of range.

= Primary input in use.

|| Secondary input in use.

c Stand-alone state; switch S1 in TEST position.

r Free running state: No input is present and no tracking has occurred. (Happens on power-up if S1 is in the RUN position and no DS1 input is present.)

b. Error conditions while in HOLD state:

2 Excess BPVs; does not cause hold.

3 LOF synchronization.

4 AIS.

5 Input in Yellow Alarm state.

6 Excessive frame bit errors (FBEs); does not cause hold.

7 Outside nominal tracking range of ±7.1 Hz or jitter more than 7 UI peak to peak.

8 Excessive invalid CRC6 codes (for ESF signals only); does not cause hold.

9 LOS (175 consecutive zeros).

c. Error conditions in Invalid Output state:

O. Overflow		Exit follow mode; unable to phase align.
U. Underflow		Input frequency is too far off.

3.3116 Card Power:
–48 volts, 1.2 amp when cold, 0.4 amp after warmup (5 minutes)

3.3117 Power Fuse:
2 amps, Type GMT

3.3118 Fuse Alarm:
Closure to battery

3.312 Model 5413 EIA RS-422 Output Driver Card

3.3121 For card layout and front panel of the Model 5413, refer to Figure 3-13.

3.3122 Input Signal:
Differential 1.544 MHz TTL clock signal from one of the two track and hold cards or, if both of these have failed, from one of the two input reference signals. The card provides for automatic selection of these input references. Automatic selection can be overridden by manual remote selection.

3.3123 Output Signals (differential TTL outputs in accordance with EIA RS-422):

List 0: 1.544 MHz square wave

List 1: 8 kHz square wave

NOTE:

The 5413 can be configured to produce a number of output frequencies. For more information, contact Larus at (800) 999-9946 toll-free or (408) 494-1500, or fax the Sales Department at (408) 494-0735.

(continued)

3.3123 (continued)

The leftmost output card produces frame synchronization for the rest of the output cards; plugging in an output card does not cause an error on another card's output.

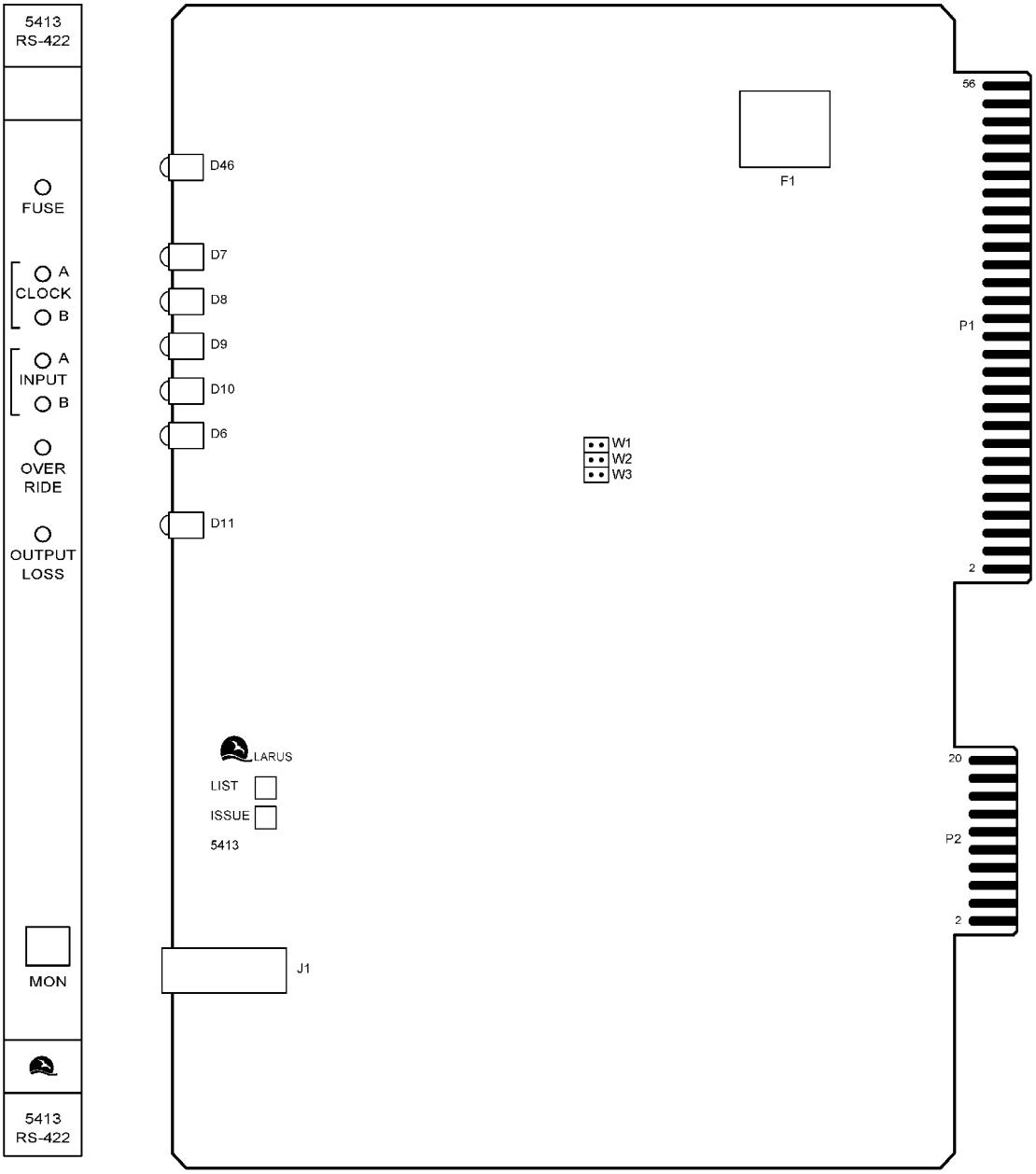


Figure 3-13. Model 5413 EIA RS-422 Output Driver Card with Front Panel

3.3124 Model 5413, Output Load Impedance:
100 ohms minimum, resistive

3.3125 Signal Amplitude:
Minimum of 2 volts peak to peak measured into a 100 ohm load

3.3126 Number of Outputs:
Ten per card; monitor jack (–20 dB) for output #1

3.3127 Output Connectors:
Wirewrap pins for up to 22 AWG shielded cable

3.3128 Output Jitter:
Less than 0.03 UI peak to peak from 10 Hz to 40 kHz

3.3129 Drive:
Each output capable of driving a differential EIA RS-422 receiver through up to 400 feet of 22 AWG office cable

3.31210 Alarms:

a. Alarm line to 5406 Alarm Interface Card signals loss of one or more outputs.

b. Alarm signal to 5405 Information Management Card.

3.31211 LED Indicators:

Front Panel Label	LED Color	Indication
FUSE	Red	Fuse alarm
CLOCK A	Green	Clock A selected
CLOCK B	Green	Clock B selected
INPUT A	Yellow	Input A selected
INPUT B	Yellow	Input B selected
OVERRIDE	Yellow	Override (manual selection)
OUTPUT LOSS	Red	Output loss

3.31212 Card Power:
–48 volts at 120 mA

3.31213 Power Fuse:
2 amps, Type GMT

3.31214 Fuse Alarm:
Closure to battery

Operation 4

4.1 General

4.101 This section consists of two parts, describing operation from the front panel and system self diagnostics. Refer to drawings of the front panels, Figures 1-3 through 1-6, in Section 1.

CAUTION:

Do not attempt operation of the STS 5400 System unless all procedures in Volume 2, Installation, Operation, and Maintenance, have been performed successfully.

4.2 Operation from Front Panel

4.201 Manual operations possible with the front panel controls include the following:

a. Hold state test on the 5402, 5403, 5410, and 5412 Track and Hold Cards.

b. Selection of clock source for the output cards.

c. Alarm cutoff (ACO) on the 5406 Alarm Interface Card.

d. Selection of the Digital Signal Level 1 (DS1) input to be monitored by the 5404 Synchronization Monitor Card.

e. Monitoring of card outputs.

4.21 Hold Mode Track and Hold Card Tests

4.211 While in operation (tracking state), the front panel TEST pushbutton will momentarily place the unit in the HOLD state without any alarms. The unit will return to the tracking state if there are no input signal problems. This tests all critical circuitry on the track and hold cards.

NOTE:

The HOLD test will only work during the Acquire 2 and DS1 tracking modes of operation. It will not work in GPS mode (5410 and 5412).

4.212 Press the TEST pushbutton until 'H' appears on the status display (this may take up to 8 seconds on the 5403). The green INPUT A (or B) light emitting diode (LED) will go off and the yellow HOLD LED will come on.

4.213 When the TEST button is released, the card will revert to normal tracking after a few seconds with the INPUT A LED on.

NOTE:

For other status display codes, refer to Section 3, Specifications, subsections 3.32, 3.33, 3.310, and 3.311.

NOTE:

STS 5400 track and hold cards are provisioned at the factory with either AA or AB input architecture. Refer to Appendix A. Assuming that there are acceptable DS1 signals at Inputs A and B:

a. For the AA input architecture, the normal reference for both track and hold cards is DS1 Input A.

b. For the AB input architecture, the normal reference for the A track and hold card is DS1 Input A and for the B track and hold card, DS1 Input B.

In the tracking state, the Input A LEDs are illuminated on both track and hold cards. References can only be changed by commands from a terminal as described in Volume 3 (TL1) or Volume 4 (Menu) User Manual.

4.22 Selection of Clock Source for Output Cards

4.221 Selection of the clock source is made from the 5405 Information Management Card.

4.222 The manual clock select mode is activated by pressing the RESET originator/recipient (O/R) button until the OVERRIDE LEDs on the 5405 and on all the output cards turn on.

4.223 Pressing the A/B CLOCK SELECT button once causes the output cards to select the next clock in the sequence CLOCK A, CLOCK B, INPUT A, INPUT B. The selection will be shown on the output card LEDs. Pressing it again will advance the sequence by one more and so on.

NOTE:

Do not leave an operational system with INPUT A or INPUT B selected unless both A and B track and hold cards have completely failed. In this state, the system has no holdover capability and does not appreciably attenuate jitter and wander on the input references.

4.224 To return to the automatic clock select state, press the RESET O/R button until the OVERRIDE LEDs turn off. If no better source is available, the system will stay where it is. If a better source is available, the system will automatically select that source. Refer to the 5400 Clock Auto-selection State Diagram, Figure 4-1.

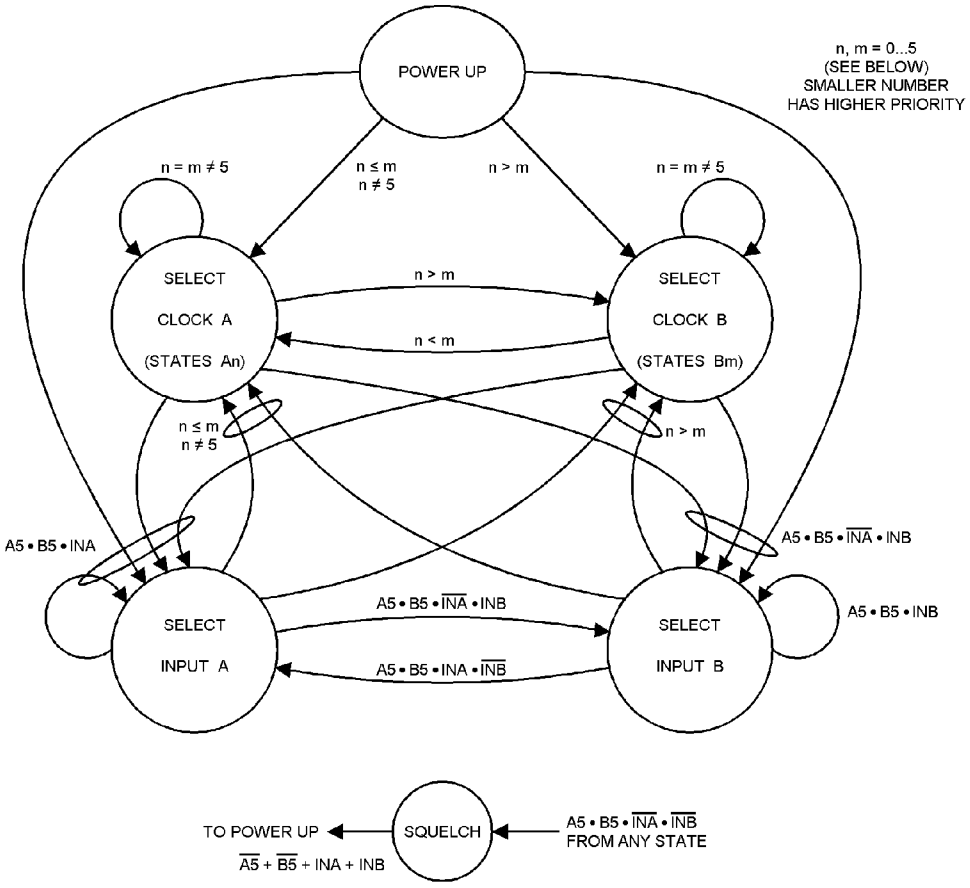
4.23 Alarm Cutoff on 5406 Alarm Interface Card

4.231 In the event of a Major or Minor alarm, the audible alarm relay contacts which connect to TB1 on the backplane can be disabled. Refer to Section 5, Figures 5-1 and 5-2.

4.232 Depress the ACO pushbutton to disable the audible alarm.

NOTE:

The yellow ACO LED will turn on but the visual alarm contacts and the LEDs will not be affected. When the alarm state is retired, the ACO LED will turn off and the audible alarm relays will be reset to respond to the next alarm.



		PRIORITY	SYMBOLS
CLOCK STATES:	ACQUIRE 2 or TRACK	1	A1, B1
	HOLD	2	A2, B2
	ACQUIRE 1 or FREE RUN or STANDALONE	3	A3, B3
	WARM UP	4	A4, B4
	FAILED	5	A5, B5
	GPS TRACK, GPS DEGRADED	0	A0, B0
INPUT DS1 SIGNAL STATES:	OK		INA, INB
	NOT OK		$\overline{INA}$, $\overline{INB}$

NOTES: + = "OR" • = "AND" $\overline{A5}$ = NOT IN STATE A5
= A1 + A2 + A3 + A4

Figure 4-1. Model STS 5400 Clock Auto-selection State Diagram

4.24 Selection of DS1 Input for 5404 Synchronization Monitor Card

4.241 The seven segment display on the 5404 card briefly shows which of the five inputs (two input references, three external inputs) is being monitored when the input is changed. Otherwise the indicator shows any bit slip between the A and B track and hold card outputs. The slip indicator rotates clockwise or counterclockwise only if the input references are different in frequency or if one of the clocks has a fault. The front panel MON INPUT jack replaces the DS1 #5 input on the backplane.

4.242 The 5404 powers up in a default mode, scanning all equipped inputs for 100 seconds each. This will show on the seven segment display.

4.243 In this scan or default mode, press the MON SELECT pushbutton once to advance the unit to the next equipped input.

4.244 Observe the front panel LEDs for any error or performance thresholds which have been exceeded for the input currently being scanned.

NOTE:

The threshold values for the 5404 LEDs are shown in Table 4-A at the end of this section. Some of these thresholds can be changed through an external terminal, as described in Volume 3, the TL1 User Manual, and Volume 4, the Menu User Manual.

4.25 Monitoring of Card Outputs

4.251 Input cards, track and hold cards, and output driver cards have monitoring jacks intended for use with a standard test set with a monitor input (100 ohms for DS1 and EIA RS-422, 130 ohms for CC, 120 ohms for E1; 20 dB standard level). The signals available are:

1. 5401 Input	Recovered DS1 A or B input reference (depending on the slot)
2. 5402/5403 Track and Hold	Framed all ones at the clock output frequency
3. 5407 DS1 Output	Framed all ones, monitoring output #1*

*Output #1 must be terminated for the monitor jacks to function correctly.

(continued)

4.25 (continued)

4. 5408 CC Output	Composite clock, monitoring output #1*
5. 5409-2 and 5409-4 E1 Output	Framed all ones, monitoring output #1*
6. 5409-3 E1 Output	2.048 MHz square wave, monitoring output #1*
7. 5410/5412 GPS Track and Hold	Framed all ones at the clock output frequency
8. 5413-0 EIA RS-422 Output	1.544 MHz square wave, monitoring output #1*
9. 5413-1 EIA RS-422 Output	8 kHz square wave, monitoring output #1*

*Output #1 must be terminated for the monitor jacks to function correctly.

4.3 STS 5400 System Self Diagnostics

4.301 The STS 5400 system has a series of software and hardware self checks as well as crosschecks between the microprocessor-controlled cards.

4.31 Model 5402, 5403, 5410, and 5412 Track and Hold Cards

4.311 A watchdog circuit monitors program execution and will restart the microprocessor if the watchdog timer is not updated.

4.312 Some failures, such as overflow in the phase correction calculation, may be caused by the input reference frequency slowly drifting out of tracking range without causing an excessive offset holdover indication. In normal operation, the input frequency of the reference will not change in this manner so overflow would represent a failure of the phase measurement circuits.

4.32 Model 5405 Information Management Card

4.321 A watchdog circuit monitors program execution and will restart the microprocessor if the watchdog timer is not updated.

4.322 The watchdog circuit also checks its serial communications ports. If a failure of any kind is detected, or if any communication channel that has been in operation is lost (e.g. a link to a track and hold card), the Information Management Card reports the alarm to the local and remote craft interfaces. If the failure is judged to be on the Information Management Card, the alarm LED lights and the 5406 Alarm Interface Card is notified.

4.323 The 5405 Information Management Card monitors alarm leads from all of the cards and will detect and report a failure on any card.

4.33 Model 5406 Alarm Interface Card

4.331 The 5406 Alarm Interface Card checks its power supply and will notify the Information Management Card and signal an alarm if failure is detected.

4.34 Model 5407, 5408, 5409, and 5413 Output Driver Cards

4.341 These cards signal an alarm if a failure of one or more of the ten outputs is detected. The alarm may be caused by a failure in circuitry on the card. As mentioned, the 5405 and 5406 both report this alarm and the affected card lights its OUTPUT LOSS LED. In order for this alarm to work properly in all cases of possible failure on the 5408 Composite Clock Card, all ten outputs must be terminated in their proper load impedance (refer to Section 3, Specifications, paragraph 3.384).

4.35 Failure Reports

4.351 Failures reported to the Information Management Card are sent over the local and remote craft interfaces with the date and time of occurrence and the cause. In TL1, unique failure reports for each of the circuit cards indicate which card to replace. Refer to Larus Practice 80-802-193, Model 5405 Information Management Card TL1 User Manual, for the format of these reports.

Table 4-A

Model STS 5400 Alarm Thresholds (Sheet 1 of 2)

5401 Input Card		
Excess bipolar violations (BPVs), error ratio approximately 10^{-4}		
5402 and 5403 Track and Hold Cards		
Alarm	**Default Threshold**	**Other Settable Threshold**
Frame Bit Errors (FBEs)	Two per second	–
Cyclic Redundancy Check (CRC) errors	16 in 10 seconds	0 to 65,535 per interval*
BPV errors	16 in 10 seconds	Same
5404 Synchronization Monitor Card		
Alarm	**Default Threshold**	**Other Settable Threshold**
Loss of Signal (LOS)	175 consecutive zeros	–
Out of Frame (OOF)	Loss of frame (LOF) synchronization for 100 milliseconds	–
BPV	16 in 10 seconds	0 to 65,535 per interval*
Invalid CRCs	Same as BPV above	Same
Time Interval Error (TIE)	36 unit intervals (UIs) in 1 hour	0 to 65,535 per interval*
Maximum Time Interval Error (MTIE)	Same as TIE above	Same
Slip	1 frame slip (193 UIs) in 1 hour	0 to 99 slips per interval*
Jitter	5 UIs peak to peak over 1 second	–

* Threshold intervals available are 1 second, 10 seconds, 1 hour, and 1 day.

Table 4-A

Model STS 5400 Alarm Thresholds (Sheet 2 of 2)

5410 and 5412 Track and Hold Cards	
Alarm	Failure Mode
GPS Antenna	Antenna power short
GPS Oscillator	GPS oscillator out of tune
GPS Input Frequency	10 MHz reference input not present
GPS 1PPS	No 1PPS
GPS Fail	10 seconds MTIE $>1.5 \times 10^{-8}$ or 1000 seconds MTIE $>3 \times 10^{-9}$ OR Degraded for twelve 10-second periods within 3 months OR Lost communications with GPS OR Still in GPS warm after 5 hours (should be GPS track) OR Estimator frequency error (EFER) data no longer good Known mode: good if sample count >7200 Position average mode: good if sample count >14,000
Alarm	Operation Mode
GPS Warm	Not tracking or failed yet
GPS Track	EFER data being used to correct direct digital frequency synthesizer (DDFS)
GPS Degraded	10 seconds MTIE $>1 \times 10^{-9}$ or 1000 seconds MTIE $>2 \times 10^{-10}$

[This page is intentionally left blank.]

Circuit Description 5

5.1 General

5.101 This section discusses the components on each card in the STS 5400 system and relates them to block diagrams. There is a block diagram for each card. A block diagram of the system is shown in Figure 1-2.

5.2 Backplane

5.201 The backplane is rack mounted in a 19/23 inch shelf. Refer to Figures 5-1 and 5-2.

5.21 Functions

5.211 The backplane receives all source signals, distributes them to the appropriate cards (J1 to J7 and J8A to J17A), and provides ten output connections (J8B to J17B) for each output card. The backplane also contains a bus for clocks and inputs. All other cards connect to the backplane.

5.22 Circuit Description

The backplane includes the following components that function as described.

5.221 Terminal Strip (TB1)

Terminal strip TB1 provides connections for fuse alarms and for major audible, minor audible, major visual, and minor visual alarms.

5.222 Terminal Strip (TB2)

TB2 supplies power and ground connection to all cards in the system.

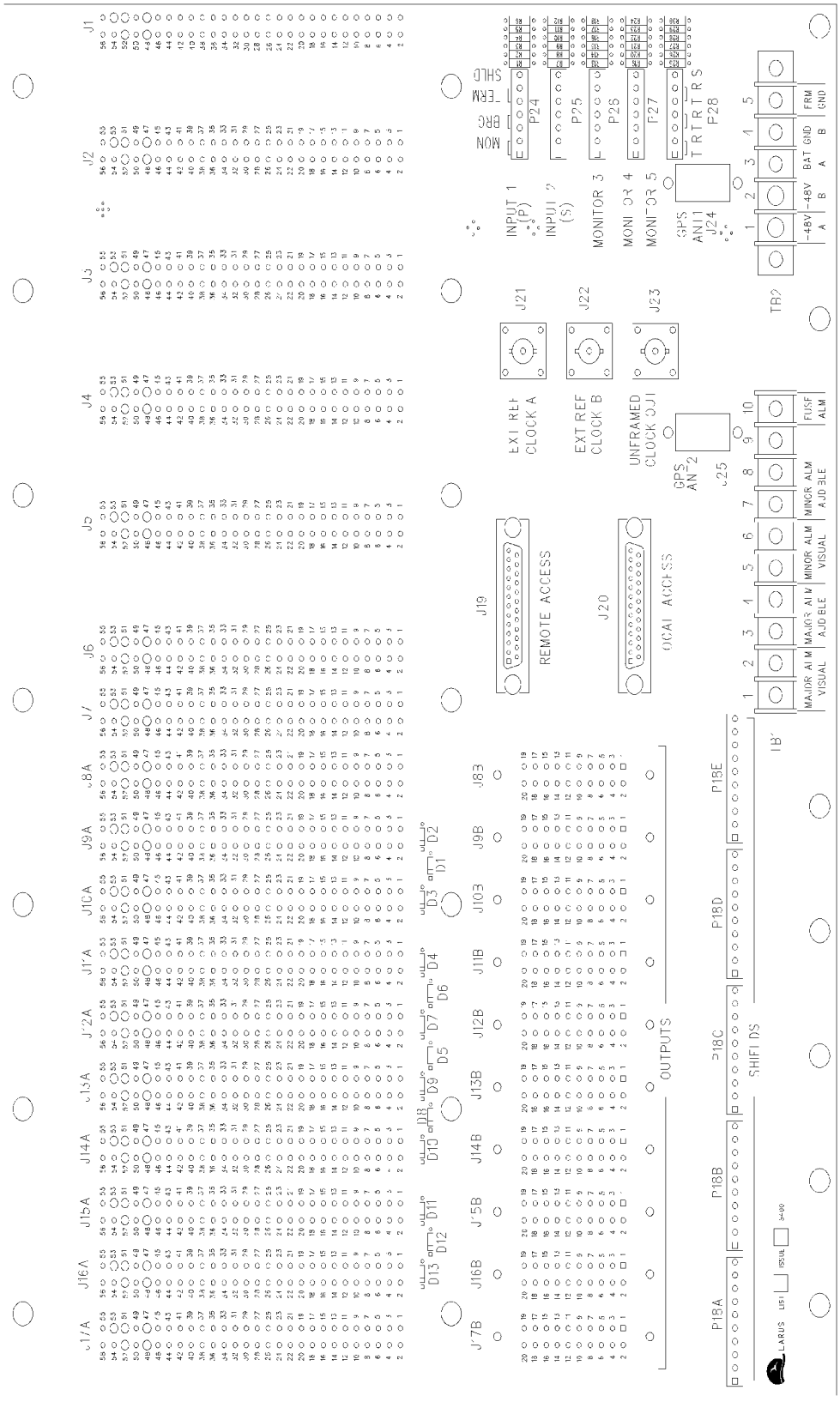


Figure 5-1. Model STS 5400-3, 5400-3A Mounting shelf Backplane (non-GPS)

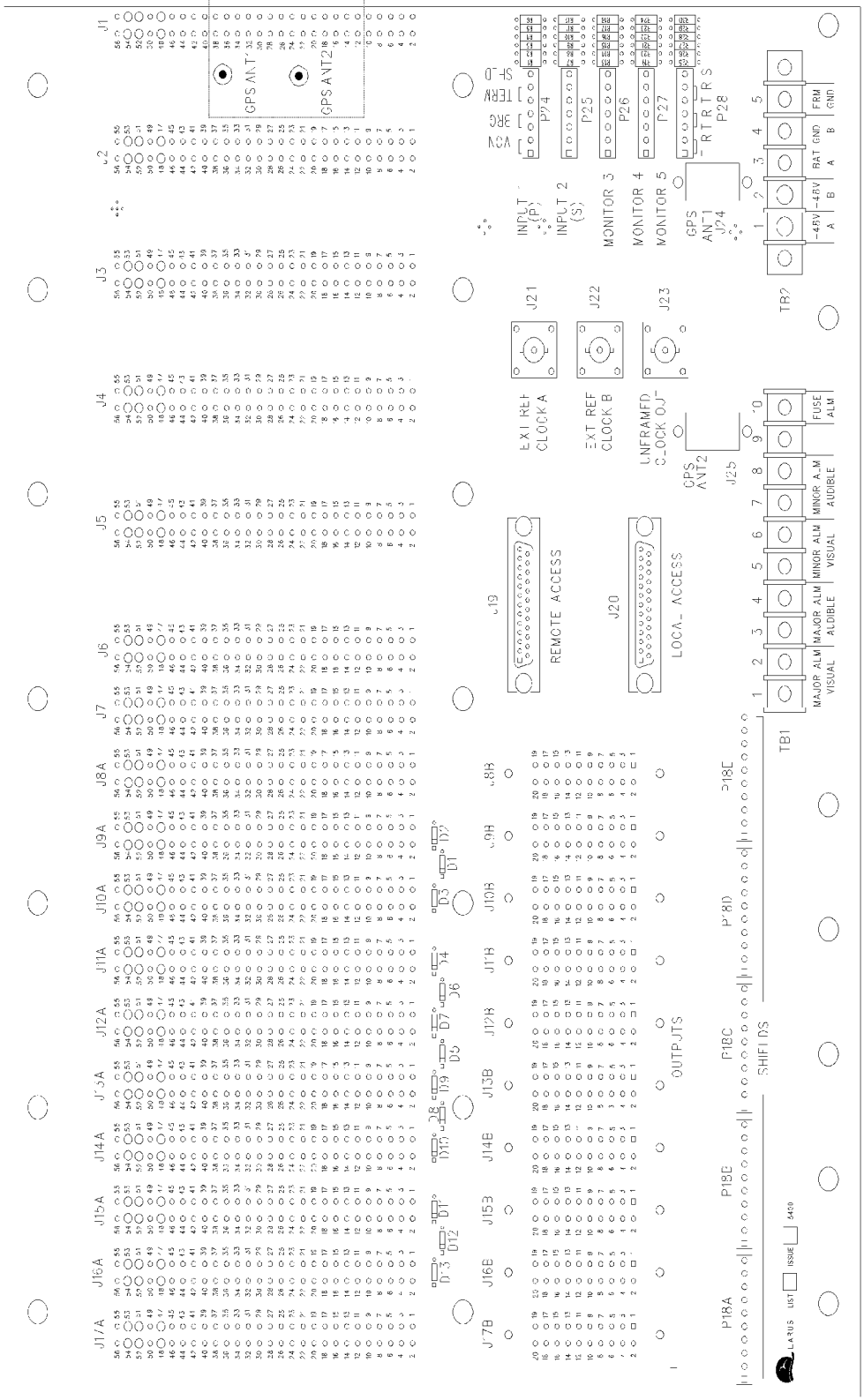


Figure 5-2. Model STS 5400-4 Mounting Shelf Backplane (GPS)

5.223 Digital Signal Level 1 Inputs (P-24 to P-28)

DS1 inputs provide three different input terminations (monitoring, bridging, and terminating) for input cards and the Synchronization Monitor Card when different pairs of 0.045 inch square wirewrap pins are selected. Shield grounds are included. The bridging and terminating inputs accept signals from 0.5 volt to 3.6 volts peak to base [18.5 to +1.6 dB digital signal crossconnect (DSX)] and the monitor input accepts signals from 0.05 volt to 0.36 volt peak to base. Input signal shields P18A to P18E provide shielded connections for the input signals if a far-end ground is not available.

5.224 External Reference Clock A (BNC J21)

BNC connector J21 gives an external 10 MHz signal for the A track and hold card.

5.225 External Reference Clock B (BNC J22)

BNC connector J22 gives an external 10 MHz signal for the B track and hold card.

5.226 Unframed Clock Out (BNC J23)

BNC connector J23 provides an isolation transformer and unframed clock monitoring for the first output card only.

5.227 Remote Access (J19)

Remote access J19 provides connection between the Information Management Card and external remote terminals through a 25-pin 'D' connector.

5.228 Local Access (J20)

Local access J20 provides connection between the Information Management Card and external local terminals through another 25-pin 'D' connector.

5.229 Diode Matrix (D1 to D13)

A diode matrix D1 to D13 determines which of the output cards is the 'master.' The master is the leftmost output card in the shelf.

5.2210 Output Pins (J8B to J17B)

Pins J8B to J17B provide ten wirewrap outputs for each output card slot.

5.2211 Card Slots (J1 to J7 and J8A to J17A)

Card slots J1 to J17A on the backplane each contain 56 pins (28 odd and 28 even). Clock and input data are bused between the various cards through these pins.

5.2212 GPS Antenna 1 (J24)

J24 (on the 5400-4 mounting shelf only) is the connector to Global Positioning System (GPS) Antenna 1. The antenna provides the L1 band (1575.42 MHz) signals with 37 dBm of gain to the GPS receiver on the A track and hold card.

5.2213 GPS Antenna 2 (J25)

J25 (on the 5400-4 mounting shelf only) is the connector to GPS Antenna 2. The antenna provides the L1 band (1575.42 MHz) signals with 37 dBm of gain to the GPS receiver on the B track and hold card.

5.3 Model 5401 DS1 Bridging Input Card

5.301 One 5401 card is used in conjunction with each 5402 or 5412 track and hold card in the Stratum 3E Enhanced or Stratum 1/3E system.

5.31 Functions

5.311 The Model 5401 DS1 Bridging Input Card performs the following functions:

a. In conjunction with circuitry on the backplane, provides terminating, bridging, and monitor inputs for the DS1 reference signal.

b. Recovers data and clock from the received signal for use by the 5402 or 5412 card.

c. Sends clock signals to the output cards.

d. Provides monitoring and alarm information to the 5406 Alarm Interface Card in the event of:

1. Loss of input signal (LOS)
2. Loss of frame (LOF)
3. Excess bipolar violations (BPVs)

5.32 Circuit Description

Refer to the 5401 DS1 Bridging Input Card block diagram, Figure 5-3, in the following discussion.

5.321 DS1 Receiver

The DS1 receiver recovers the data and clock from the DS1 input reference. The recovered clock and data are fed to the Receive Framer (RCV FRMR) from a +20 dB amplifier. The RCV FRMR tests for certain input error conditions. The recovered clock and data signals are also passed to output buffers.

The DS1 receiver chip recovers the clock and data from the input signal. The clock recovery oscillator in the receiver is synchronized to the amplified and full-wave rectified input signal. The oscillator tracks the input bit rate exactly, as long as excessively lengthy sequences of zeros (more than 15 consecutive zeros) do not occur.

The DS1 receiver outputs the data in dual rail format, one output that represents positive voltage excursions and another for negative voltage excursions of the input.

5.322 Receive Framer

The framer receives the clock and data signal from the DS1 receiver and tests for various signal conditions. The framer drives front panel light emitting diodes (LEDs) which indicate the following signal conditions:

a. The green PULSES LED is on if the average pulse density is one in eight or greater.

b. The yellow INPUT FAULT LED indicates a BPV error ratio of about 10^{-4} or worse.

c. The red LOS LED indicates either a loss of signal (more than 175 ±75 consecutive zeros) or an out of frame (OOF) condition caused by an alarm indication signal (AIS).

For AIS, the PULSES LED will be on. In the event of a complete LOS, the PULSES LED will be off.

The LOS condition results in a card alarm output on pin 44 to the 5406 Alarm Interface Card and to the 5405 Information Management Card.

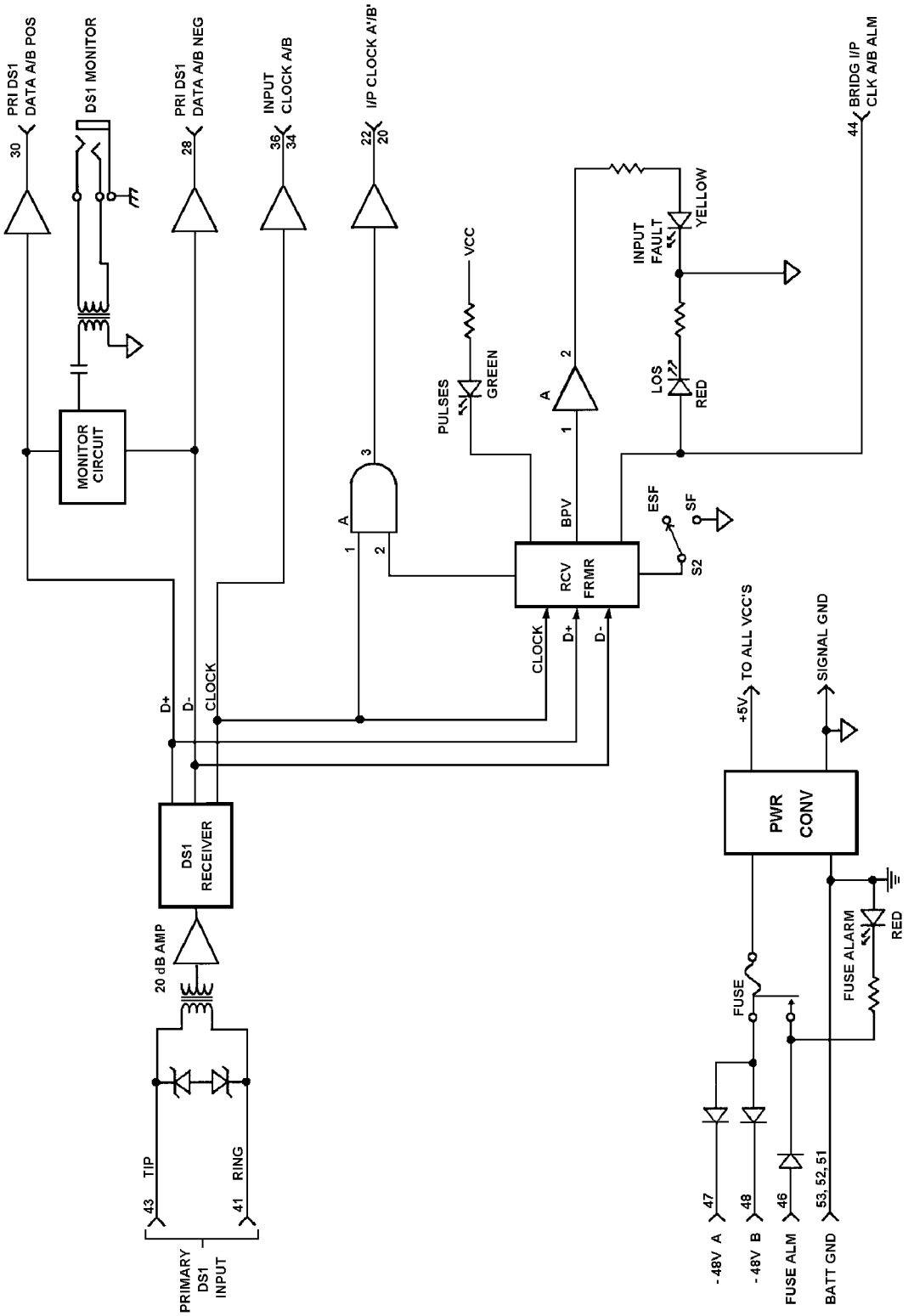


Figure 5-3. Model 5401 DS1 Bridging Input Card

5.323 Output Data

The dual rail data and recovered clock are sent to both 5402 or 5412 track and hold cards via backplane buses. The recovered clock is also sent on another bus to all output cards for use if both track and hold cards should fail.

5.324 Monitor Jack

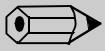
A front panel jack allows the recovered signal to be monitored by any DS1 test set with a monitor input (–20 dB referenced to the DSX-1).

5.325 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.4 Model 5402 DDFS Stratum 3E Enhanced Track and Hold Card

5.401 There are two 5402 direct digital frequency synthesizer (DDFS) cards in a redundant Stratum 3E Enhanced system. The 5402-3 supports the AB input architecture; the 5402-4 supports the AA input architecture.



NOTE:

Both track and hold cards in a system must support the same input architecture, either AA or AB. See Appendix A.

5.41 Functions

5.411 The Model 5402 DDFS Stratum 3E Enhanced Track and Hold Card performs the following functions:

a. Accepts one of two 1.544 MHz DS1 data and clock signals and provides a smoothed and jitter free signal to the output cards from a synthesizer tracking the input reference.

b. Monitors its reference input for framing and cyclic redundancy check sum (CRC6) errors. An out-of-specification input signal forces the card to hold to the last known reference, with a drift of less than $5x10^{9}$ in 24 hours. The signal to the output cards is continuous (no phase hits) during any switch from track to hold. Frequency and phase corrections

5.411 (continued)

occur over periods of about 3000 seconds. A fast ACQUIRE state reduces this to 100 seconds for power-up and 300 seconds when returning from the HOLD state.

c. Accepts an alternate external 10 MHz signal from a high stability timing source such as a GPS receiver, cesium clock, or similar mechanism. This signal may be used to replace the 10 MHz reference from the on-board precision oscillator or as a tracking input. The external 10 MHz signal is selected as a reference by on-card switches/jumpers. It is selected as a tracking reference through user commands to the 5405 Information Management Card.

d. Supplies monitoring and alarm information to the 5405 and 5406 cards.

5.42 Circuit Description

Refer to the block diagram in Figure 5-4 in the following discussion.

5.421 DS1 Input

The 5402 card gets its DS1 inputs, data, and clock from the 5401 Input Card. It selects either the A or B input reference DS1 signal via the analog switch. Assuming that there are acceptable DS1 signals at DS1 Inputs A and B:

a. For the AB input architecture, the primary reference for the A track and hold card is DS1 Input A and for the B track and hold card it is DS1 Input B.

b. For the AA input architecture, the primary reference for both track and hold cards is DS1 Input A. In this state, the Input A LED is illuminated on both track and hold cards.

Input references can only be changed by commands from a terminal as described in the Volume 3 (TL1) or Volume 4 (Menu) STS 5400 User Manual.

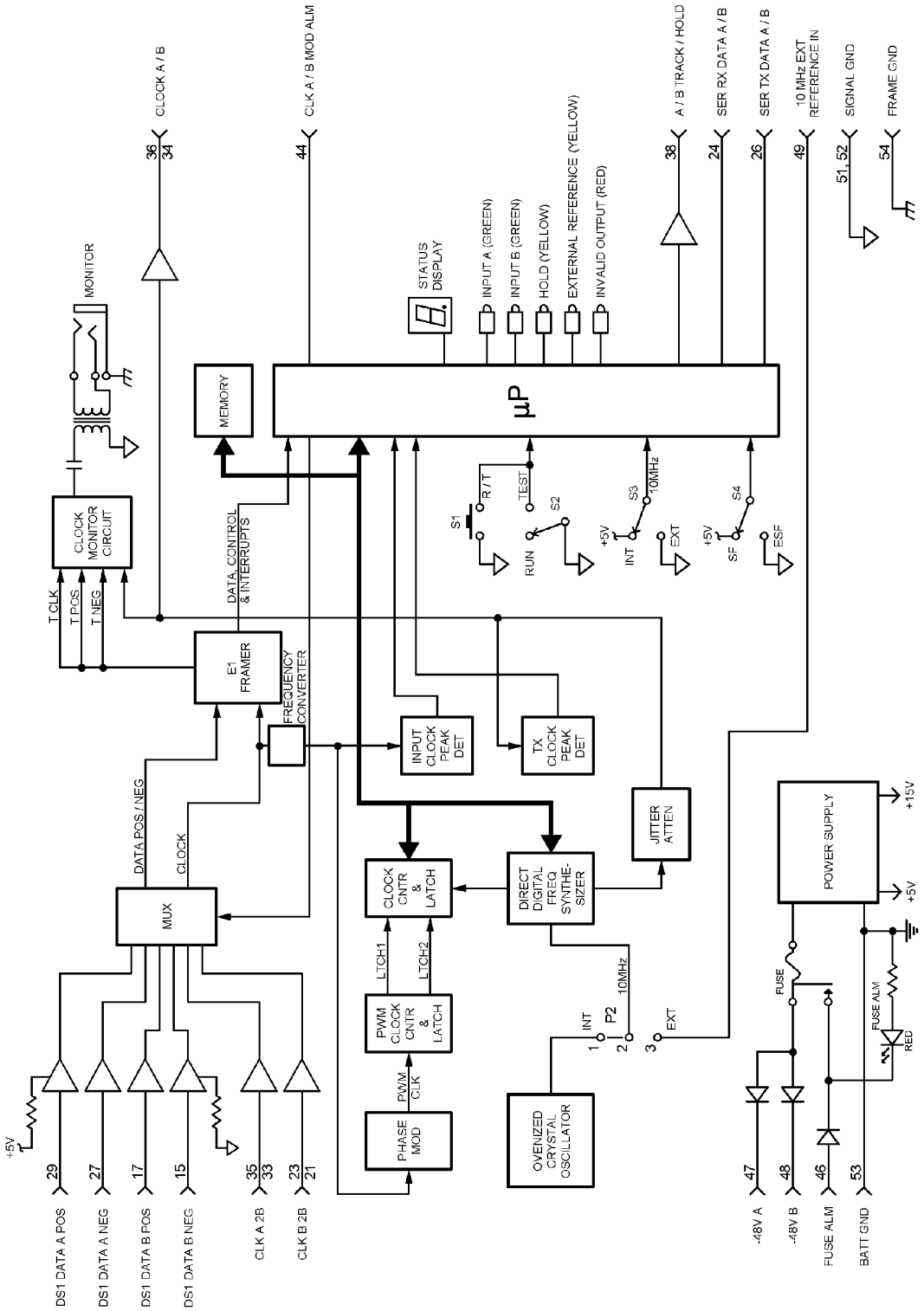


Figure 5-4. Model 5402 DDFS Stratum 3E Enhanced Track and Hold Card

5.422 DS1 Receiver

The 5402 DS1 receiver regenerates the selected incoming signal and recovers both the clock and the data. The data go to the framing circuit. The 5402 measures the input DS1 reference bit time phase as compared to the ovenized crystal oscillator output by means of a digital phase detector. Samples of phase information are collected and averaged, over about a one-second period, to provide input to the control algorithm. If, at any point in the accumulation and calculation period, a condition is detected (excessive errors, LOS, LOF, etc.) which causes the collected information to be suspect, the unit enters the holdover state and does not update the correction to the oscillator. If the data are qualified, then the update will proceed. After 128 acquire cycles (about 2 minutes) following initial qualification, the clock will be in the tracking mode. After 5 to 7 minutes, the tracking mode will be at minimum error if the input is within specifications. The 5402 will track timing signals from any other Stratum 3 or higher source (i.e., Stratum 2 or 1) having a frequency offset of no more than ±7.1 Hz.

5.423 Framer

The framing circuit detects the following framing errors:

a. Yellow Alarm, LOS (175 ±75 consecutive zeros)

b. BPVs

c. Invalid CRC6 codes [extended superframe (ESF) framing only]

An impaired signal causes the microcontroller to cease tracking, go into the HOLD mode, and indicate the type of impairment on the seven segment display.

5.424 Ovenized Crystal Oscillator

A 10 MHz ovenized crystal oscillator provides the input to a 48-bit DDFS.

5.425 Direct Digital Frequency Synthesizer

The oscillator is coupled to the DDFS and acts as a reference for it. The DDFS operates on the presumption that oscillator frequency is kept within a reasonable degree of precision, e.g. within one part in 10^{+8}. The DDFS uses a digital process to convert the signal from the oscillator into a signal having a second related frequency. The DDFS accomplishes this conversion by utilizing a stored algorithm and a numerical input from the microprocessor.

(continued)

5.425 (continued)

The DDFS accepts an integer, N, from the microprocessor. The DDFS then generates a new output frequency 'F out' from 'F osc' according to the following formula:

$$F\ out = \frac{(N)\ (F\ osc)}{2^{48}}$$

where 48 is the number of binary digits (bits) used by the DDFS and (F osc) is nominally 10 MHz.

Input to the microprocessor is the relative phase of the DDFS output and the input signal. Software computes phase deviation from initial reference and rate of change of phase difference. These parameters are used to compute an adjustment to the integer (N) which controls the DDFS. The hardware/software combination constitutes a discrete implementation of a second-order linear control loop (Δ T is 1.3 seconds). The step-response of such a system is a function of the difference of two exponential terms which are the time constants. There is a pair of time constants for each of ACQUIRE 1, ACQUIRE 2, and normal tracking. The primary (shorter) time constant is the dominant factor in determining initial behavior.

The control loop of the 5402 is piece-wise linear, since normal and ACQUIRE 2 can alternate.

5.426 Controls and Latches

The output phase is compared with the phase of the recovered input reference clock by means of a pair of counters and latches, good signal or bad:

a. When the input signal is deemed good, the microcontroller tracks the input phase and, approximately once per second, calculates a new 48-bit control word for the DDFS based on the input/output phase difference and rate of change. The 16 most significant bits (MSBs) of the control word are fixed and the microcontroller calculates the 32 least significant bits (LSBs).

b. When the input is deemed bad, tracking ceases (HOLD mode). Any fault which triggers the HOLD state saves the last known good output frequency correction factor and uses it to determine the HOLD frequency.

5.427 Controls and Indicators

The following controls and indicators appear on the front panel of the 5402 card:

a. The red FUSE LED indicates an internal fuse has blown.

b. The green INPUT A/B LEDs indicate which of the two input signals the card is tracking.

c. The first yellow LED indicates that the unit is in the HOLD mode.

d. The second yellow LED indicates that the 10 MHz EXTERNAL REFERENCE input is in use.

e. The red LED indicates INVALID OUTPUT due to a failure condition on the card.

f. The seven segment display indicates the STATUS of the output failure.

g. The TEST pushbutton causes the microcontroller to execute a diagnostic routine and display 'H' if successful. The unit returns to normal tracking in a few seconds.

5.428 Alarm Output

The HOLD or INVALID OUTPUT condition, or a fault reported by the crystal oscillator, results in a card alarm output to the 5406 Alarm Interface Card and to the 5405 Information Management Card. A data link to the 5405 card allows the 5402 card to report its status (tracking, hold, stand-alone, or failed).

5.429 Clocks A and B

Each of the two 5402 cards in a normal redundant system drives a Clock A or B differential 1.544 MHz bus to the ten output card slots. Each 5402 also drives a hold indicator bus. Selection of the A or B clock is done automatically by logic circuitry on the output cards; it can be changed manually from a terminal connected to the 5405 Information Management Card.

5.4210 Phase Detector

The phase detector adjusts the phase of the slave 5402 card (normally Clock B) to match the phase of the master 5402 (normally Clock A). Thus, there is no phase hit during a switch from Clock A to Clock B and vice versa.

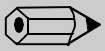
5.4211 External 10 MHz Signal

The external 10 MHz signal input is intended for an external reference oscillator in place of the 'ON CARD' oscillator. Such a signal could come from a cesium clock, a GPS or LORAN C receiver, or similar source.

The external 10 MHz signal may be selected as the reference to the DDFS in place of the on-board 10 MHz precision oscillator by the appropriate setting of on-board switches/jumpers. When the external 10 MHz signal is selected for this purpose, the EXTERNAL REFERENCE LED will light when a 10 MHz reference signal and a DS1 input signal are present.

If the external 10 MHz reference is selected and is not present, the track and hold card will not provide an output to its clock bus but will go into the ALARM state. The front panel INVALID OUTPUT LED will light. If there is no other track and hold card in the system, the output driver card(s) will select one of the two DS1 inputs to output. If, under this condition, the DS1 input is not present or fails, a false signal will be present at the output. This signal will be delivered to the output driver card(s) and will appear on the system outputs. This is NOT a valid signal. The system will be indicating multiple failures and sending notifications from the 5405 Information Management Card to user terminals.

The external 10 MHz signal may also be selected as a tracking input in place of the DS1 inputs. Selection is done by TL1 or Menu User commands through the interfaces of the 5405 Information Management Card. If the external 10 MHz signal is selected as a tracking input and is not present, the track and hold card will go into holdover mode and light the HOLD LED on its front panel. The output driver cards will switch to use the signal from the other track and hold card, if present, or one of the two DS1 inputs.



NOTE:

It is possible to select the external 10 MHz signal as both an external reference and a tracking input at the same time but this is not a valid mode of operation.

5.4212 Monitor Jack

A front panel DS1 monitor jack (–20 dB referenced to the DSX-1) provides framed all ones at the clock output frequency.

5.4213 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.5 Model 5403 Stratum 2 Track and Hold Card

5.501 There are two 5403 cards in a redundant Stratum 2 system. The 5403-3 supports the AB input architecture; the 5403-4 supports the AA input architecture.

NOTE:

Both track and hold cards in a system must support the same input architecture, either AA or AB. See Appendix A.

5.51 Functions

5.511 The Model 5403 Stratum 2 Track and Hold Card performs the following functions:

a. Accepts one of two 1.544 MHz DS1 reference signals, extracts its timing, and provides a smoothed and jitter free signal to the output cards from a rubidium oscillator tracking the input reference.

b. Monitors its reference input for framing and CRC6 errors. An out-of-specification input signal forces the unit to hold to the last known reference, with a drift of less than 7.5×10^{-11} in 24 hours. By means of a digital phase detector, the 5403 measures the input DS1 reference bit time phase compared to the rubidium atomic oscillator output as conditioned by a DDFS. Samples of phase information are collected and averaged over about a seven-second period to provide input to the control algorithm. If, at any point in the accumulation and calculation period, a condition is detected (excessive errors, LOS, LOF, etc.) which causes the collected information to be suspect, the unit enters the holdover state and does not update the correction to the synthesizer. If the data are qualified, then the update will proceed. After 128 acquire cycles (about 15 minutes) following initial qualification, the clock will be in the tracking mode. After 45 to 60 minutes, the tracking mode will be at minimum error if the input is within specifications. The 5403 will track timing from another Stratum 2 or Stratum 1 source having an average frequency offset of no more

(continued)

5.511 Model 5403, Functions (continued)

than ±0.04 Hz. The signal to the output cards is continuous (no phase hits) during any switch from track to hold. Frequency and phase corrections occur over periods of about 10,000 seconds. A fast ACQUIRE state reduces this to 300 seconds for power-up and 1000 seconds for return from the HOLD state.

c. Accepts an alternate external 10 MHz signal from a high stability timing source such as a GPS receiver, cesium clock, or similar mechanism. This signal may be used to replace the 10 MHz reference from the on-board precision oscillator or as a tracking input. The external 10 MHz signal is selected as a reference by on-card switches/jumpers. It is selected as a tracking reference through user commands to the 5405 Information Management Card.

d. Supplies monitoring and alarm information to the 5405 and 5406 cards.

5.52 Circuit Description

Refer to the block diagram in Figure 5-5 in the following discussion.

5.521 DS1 Input

The 5403 card has its own DS1 input circuits and does not require a separate input card. It selects either the A or B input reference DS1 signal via the analog switch. Assuming that there are acceptable DS1 signals at DS1 Inputs A and B:

a. For the AB input architecture, the primary reference for the A track and hold card is DS1 Input A and for the B track and hold card, it is DS1 Input B.

b. For the AA input architecture, the primary reference for both track and hold cards is DS1 Input A. In this state, the Input A LED is illuminated on both track and hold cards.

The references can only be changed by commands from a terminal as described in the Volume 3 (TL1) or Volume 4 (Menu) STS 5400 User Manual. This should only be done to provide temporary backup in the event that one input has failed and cannot be fixed for an extended period of time. In all normal operating modes, the track and hold cards should be tracking their corresponding inputs.

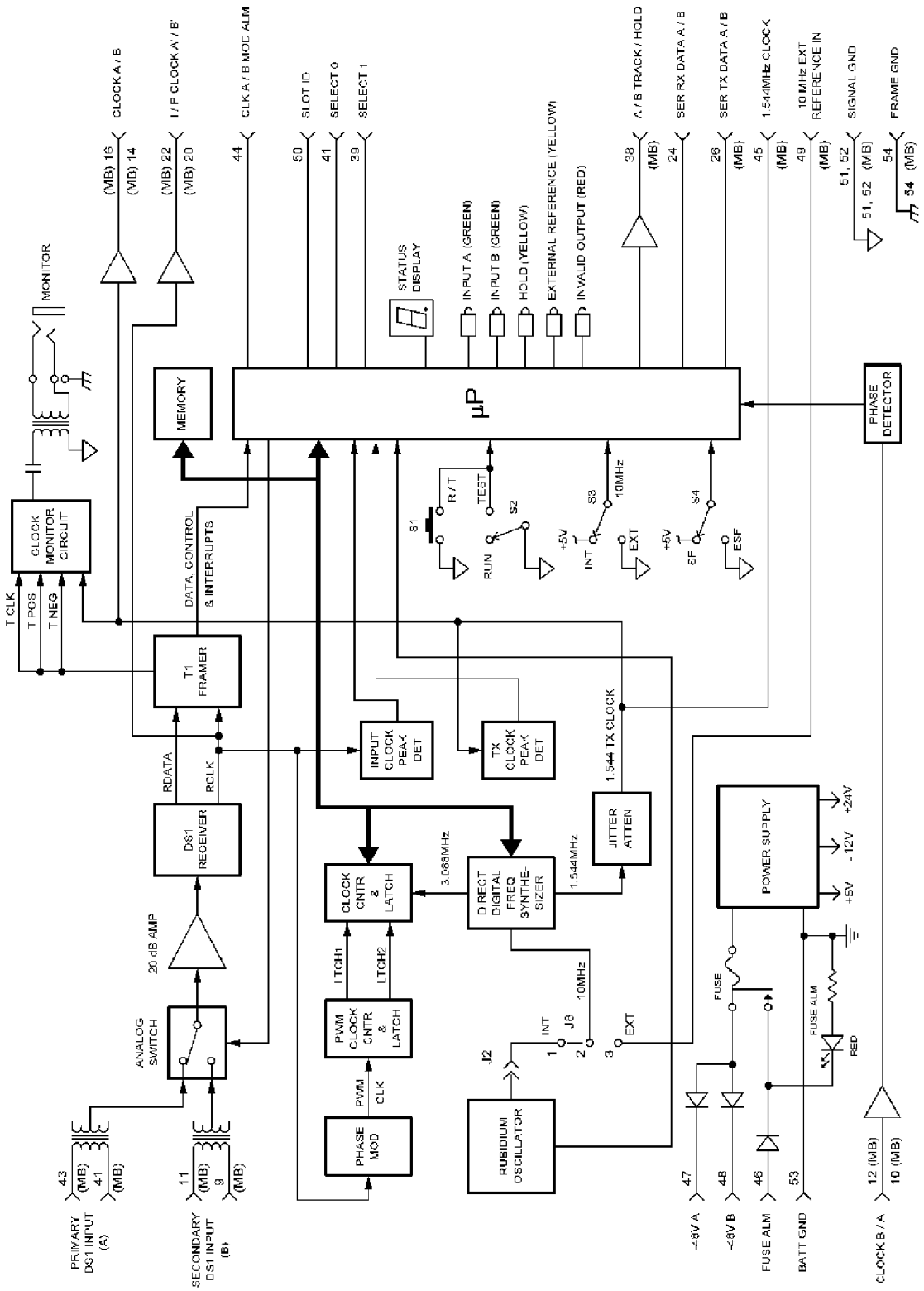


Figure 5-5. Model 5403 Stratum 2 Track and Hold Card

5.522 DS1 Receiver

The 5403 DS1 receiver regenerates the selected incoming signal and recovers both the clock and the data. The data go to the framing circuit.

5.523 Model 5403, Framer

The framing circuit detects the following framing errors:

a. Yellow Alarm, LOS (175 ±75 consecutive zeros)

b. BPVs

c. Invalid CRC6 codes (ESF framing only)

An impaired signal causes the microcontroller to cease tracking, go into the HOLD mode, and indicate the type of impairment on the seven segment display.

5.524 Rubidium Oscillator

A 10 MHz rubidium oscillator provides the input to a 48-bit DDFS.

5.525 Direct Digital Frequency Synthesizer

The oscillator is coupled to the DDFS and acts as a reference for it. The DDFS operates on the presumption that oscillator frequency is kept within a reasonable degree of precision, e.g. within one part in 10^{+9}. The DDFS uses a digital process to convert the oscillator signal into a signal having a second related frequency. The DDFS accomplishes this conversion by utilizing a stored algorithm and a numerical input from the microprocessor.

The DDFS accepts an integer, N, from the microprocessor. The DDFS then generates a new output frequency 'F out' from 'F osc' according to the following formula:

$$F\ out = \frac{(N)\ (F\ osc)}{2^{48}}$$

where 48 is the number of bits used by the DDFS and (F osc) is nominally 10 MHz.

Comments about the control loop in paragraph 5.425 also apply to the 5403. The main difference (other than time constants and Δ T being 8 seconds) is that normal tracking does not revert to ACQUIRE 2 directly.

5.526 Model 5403, Controls and Latches

The output phase is compared with the phase of the recovered input reference clock by means of a pair of counters and latches, good signal or bad:

a. When the input signal is deemed good, the microcontroller tracks the input phase and, every 7 seconds, calculates a new 48-bit control word for the DDFS based on the input/output phase difference and rate of change. The 24 MSBs of the control word are fixed and the microcontroller calculates the 24 LSBs.

b. When the input is deemed bad, tracking ceases (HOLD mode). Any fault which triggers the HOLD state saves the last known good output frequency correction factor and uses it to determine the HOLD frequency.

5.527 Controls and Indicators

The following controls and indicators appear on the front panel of the 5403 card:

a. The red FUSE LED indicates an internal fuse has blown.

b. The green INPUT A/B LEDs indicate which of the two input signals the card is tracking.

c. The first yellow LED indicates that the unit is in the HOLD mode.

d. The second yellow LED indicates that the 10 MHz EXTERNAL REFERENCE input is in use.

e. The red LED indicates INVALID OUTPUT due to a failure condition on the card.

f. The seven segment display indicates STATUS of the output failure.

g. The TEST pushbutton causes the microcontroller to execute a diagnostic routine and display 'H' if successful. The unit returns to normal tracking in a few seconds.

5.528 Model 5403, Alarm Output

The HOLD or INVALID OUTPUT condition, or a fault reported by the rubidium oscillator, results in a card alarm output to the 5406 Alarm Interface Card and to the 5405 information Management Card. A data link to the 5405 card allows the 5403 card to report its status (tracking, hold, stand-alone, or failed).

5.529 Clocks A and B

Each of the two 5403 cards in a normal redundant system drives a Clock A or B differential 1.544 MHz bus to the ten output card slots. Each 5403 also drives a hold indicator bus. Selection of the A or B clock is done automatically by logic circuitry on the output cards.

5.5210 Phase Detector

The phase detector adjusts the phase of the slave 5402 card (normally Clock B) to match the phase of the master 5402 (normally Clock A). Thus, there is no phase hit during a switch from Clock A to Clock B and vice versa.

5.5211 External 10 MHz Signal

The external 10 MHz signal input is intended for an external reference oscillator in place of the 'ON CARD' oscillator. Such a signal could come from a cesium clock, a GPS or LORAN C receiver, or similar source.

The external 10 MHz signal may be selected as the reference to the DDFS in place of the on-board 10 MHz precision oscillator by the appropriate setting of on-board switches/jumpers. When the external 10 MHz signal is selected for this purpose, the EXTERNAL REFERENCE LED will light when a 10 MHz reference signal and a DS1 input signal are present.

If the external 10 MHz reference is selected and is not present, the track and hold card will not provide an output to its clock bus but will go into the ALARM state. The front panel INVALID OUTPUT LED will light. If there is no other track and hold card in the system, the output driver card(s) will select one of the two DS1 inputs to output. If, under this condition, the DS1 input is not present or fails, a false signal will be present at the output. This signal will be delivered to the output driver card(s) and will appear on the system outputs. This is NOT a valid signal. The system will be indicating multiple failures and sending notifications from the 5405 Information Management Card to user terminals.

5.5211 Model 5403, External 10 MHz Signal (continued)

The external 10 MHz signal may also be selected as a tracking input in place of the DS1 inputs. Selection is done by TL1 or Menu user commands through the interfaces of the 5405 Information Management Card. If the external 10 MHz signal is selected as a tracking input and is not present, the track and hold card will go into holdover mode and light the HOLD LED on its front panel. The output driver cards will switch to use the signal from the other track and hold card, if present, or one of the two DS1 inputs.

NOTE:

It is possible to select the external 10 MHz signal as both an external reference and a tracking input at the same time but this is not a valid mode of operation.

5.5212 Monitor Jack

A front panel DS1 monitor jack (–20 dB referenced to the DSX-1) provides framed all ones at the clock output frequency.

5.5213 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.6 Clock Operation, 5402 and 5403 Cards

5.601 The 5402 Stratum 3E Enhanced and 5403 Stratum 2 Track and Hold Cards have similar algorithms that differ only in the constants assigned for:

number of samples of the phase (ACQ_OUT)
multiplier for the error from start of tracking (DIF_MUL)
multiplier for the error between phase accumulations (DEL_DIF)
damping factor for loop response (DAMP)
long-term averaging factor (LONGAVG)

5.602 The constants for both clocks are the same except for the phase accumulation, or number of samples of the phase, which is 128 for the 5402 Stratum 3E Enhanced and 32,768 for the 5403 Stratum 2.

5.603 The accumulated phase takes about 0.5 seconds to calculate on the Stratum 3E Enhanced and 7 to 8 seconds on the Stratum 2. The accuracy of the phase calculation of the Stratum 3E Enhanced is 1/4 UI or 162 nanoseconds. Accuracy of the phase calculation on the Stratum 2 is better than 0.04 nanosecond due to a dither circuit that extends the accuracy of the phase measurement logic. The calculation is performed as follows:

a. The clocks start out by taking a phase measurement, which is the average phase difference between the clock's output and the reference input. This first reading acts as a signpost for the algorithm. The clock will attempt to keep the output close to the input phase as represented by this first reading.

b. Another reading is taken and compared with the first. This difference is the error in phase between the input and the output. This first difference may be seen as representing the position error of the phase.

c. A calculation of the difference of two successive readings is taken. This calculation expresses the rate of change of the phase and may be seen as representing the velocity error of the phase.

d. The first difference is multiplied by a scale factor and added to the second difference multiplied by another scale factor. This is called the correction factor. The correction factor represents the scaled error from the correct phase as well as a value that expresses how fast the correct phase is being departed from or approached.

e. The control value to be sent to the DDFS is then calculated by taking the last long-term average of the control values, adding the latest successive average of the control value and the correction, times the damping value, less the last control value, and dividing by the long-term average sample number.

f. The long-term average is formed by taking old control values and averaging them into another damped response summation to yield the long-term average control value.

g. The algorithm returns to take another reading and repeat the above. If, before the control value is to be updated at the DDFS, there has been a condition that requires the clock to go into holdover, the control value is not updated from its last value and the unit goes into holdover. Once the condition has cleared, the algorithm proceeds from the top by taking a new first reading.

5.604 Thus the value used for control prior to holdover represents a damped average of the short-term corrections and the long-term offset average. The time taken for this process is about 2 minutes for the Stratum 3E Enhanced clock and about 15 minutes for the Stratum 2 clock. Complete stability and convergence may take as long as 4.5 hours for the Stratum 3E Enhanced and 32 hours for the Stratum 2. These times are based on the worst case long-term average offset, which is not normally present. Typical times are 30 minutes for the Stratum 3E Enhanced clock and 3.5 hours for the Stratum 2 clock.

5.7 Model 5404 Synchronization Monitor Card

5.701 The 5404 card is a DS1 performance measurement device.

5.71 Functions

5.711 The Model 5404 Synchronization Monitor Card performs the following functions:

a. Measures the performance of the two reference DS1 inputs or any of three external DS1 signals using the currently selected track and hold card output as a standard.

b. Measures time interval error (TIE), maximum time interval error (MTIE), bit and frame slips, peak to peak wideband jitter (above 10 Hz), and peak to peak wander over the selected observation interval. TIE, MTIE, and wander are calculated from phase data processed through a 10 Hz low-pass filter.

c. Determines DS1 performance parameters of any one of the five signals in item a. above (refer to Section 3, Specifications, paragraph 3.345).

d. Selects observation intervals of 1, 10, 100, 1000, 10,000, and 100,000 seconds for any of the five inputs. In an alternative mode, the 5404 acquires 32 samples of unfiltered phase data over the selected observation interval for any of the five inputs. Any single input can be monitored indefinitely.

e. Selects scan mode which will accumulate data from all five of the inputs sequentially. The default scan mode is for 100 seconds on each input in turn. The 5404 is directed by the 5405 Information Management Card to measure one or more of the inputs in one of its modes. Refer to the TL1 User Guide, Larus Practice 80-802-193, for information on all of the modes.

f. Independently compares the two track and hold card outputs for bit slip.

(continued)

5.711 (continued)

g. Reports performance and alarms through the 5405 Information Management Card to remote or local terminals. Alarm states are shown on front panel LED indicators.

5.72 Circuit Description

The 5404 block diagram appears in Figure 5-6. Refer also to Section 3, Specifications, paragraph 3.345, for a detailed description of the measurements that this card performs.

5.721 Input Select Switch and Input Select Switch Decoder

The input select switch selects primary, secondary, or one of the three external inputs for performance monitoring under microprocessor control of the input select switch decoder (ISSD).

5.722 DS1 Receiver

The DS1 receiver recovers clock and data from the selected input after a 20 dB amplifier.

5.723 Receive Framer

Clock and data are fed to the framer chip, which is periodically read by the microprocessor to obtain counts of LOS events, OOF events, BPVs, and CRC6 code errors. This information is sent to the 5405 card for storage and later reporting and, if any counts exceed certain thresholds (refer to Table 4-A), the corresponding front panel yellow LED is turned on.

5.724 Phase Detectors

Recovered clock from the DS1 being monitored is sent to phase detectors for time interval measurements. The other input (reference) to the phase detectors is the same clock that is currently selected by the output driver cards.

The fine phase detector determines the time interval difference within a single unit interval (648 nanoseconds) with an 8-bit resolution.

The coarse phase detector comprises two 8192-bit counters and a data latch. It determines time interval differences (from an arbitrary starting point) of up to ± 4096 unit intervals (2.6 milliseconds = 20 frames).

(continued)

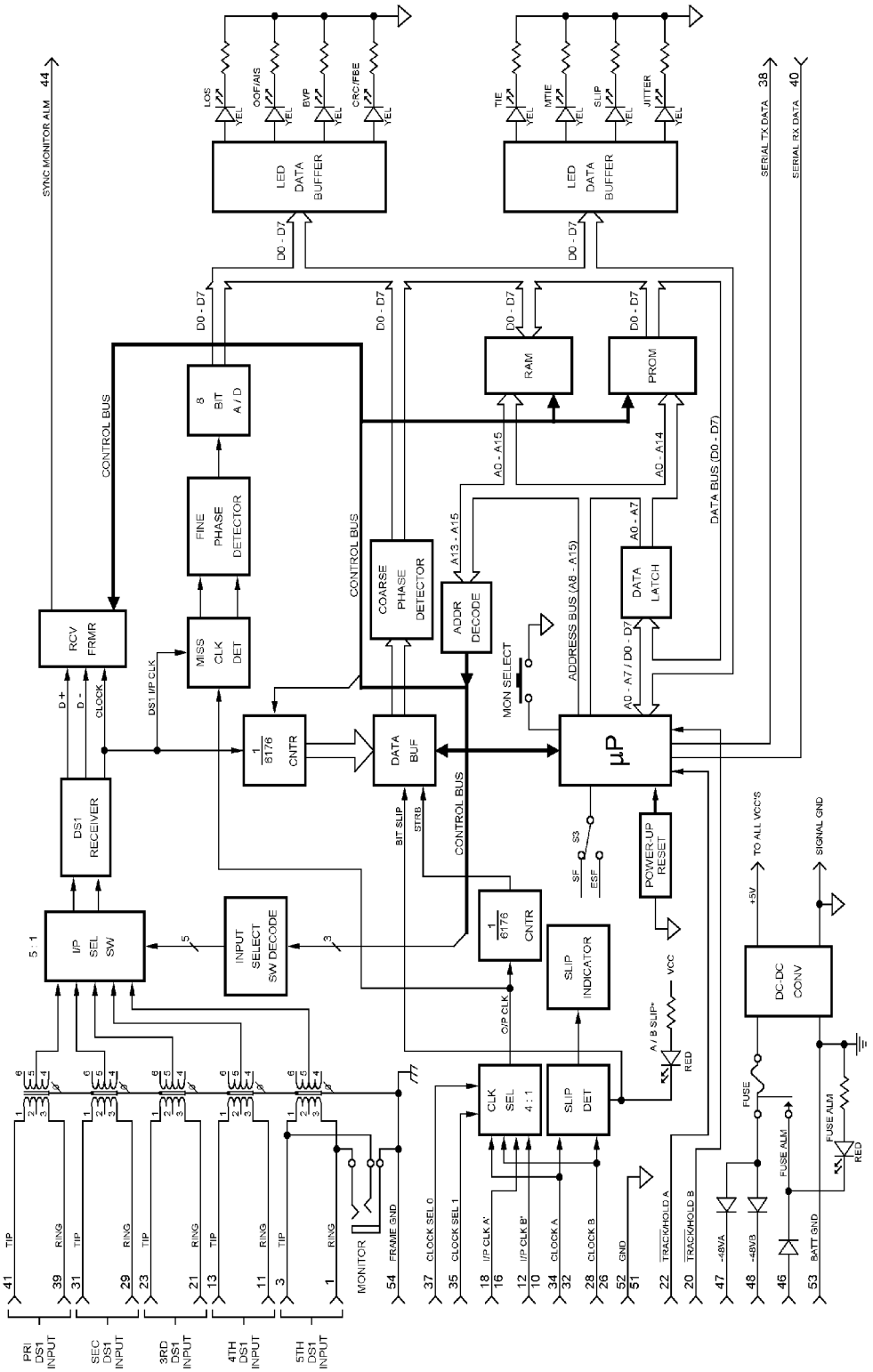
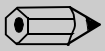


Figure 5-6. Model 5404 Synchronization Monitor Card

5.724 Model 5404, Phase Detectors (continued)

The hardware phase sampling rate is approximately 188 per second. The coarse and fine phase information is combined into phase samples displayed in nanoseconds. The fine phase detector interpolates between the coarse phase detector's one unit interval resolution measurements to obtain finer resolution. The fine phase detector has one RS flip-flop which is set by the leading edge of the reference clock and reset by the leading edge of the clock to be measured. The output pulse width is thus proportional to the time (phase) difference between these two clock edges. The output pulses are averaged by an RC filter of about 60 microseconds time constant. The averaged output voltage ranges from nearly zero volts for nearly zero phase difference to nearly 5 volts for nearly 646 nanoseconds (one unit interval) phase difference. This averaged voltage is delivered to one 8-bit analog/digital (A/D) converter with a built-in sample-and-hold circuit. The converter is set up so that inputs between 0 and 5 volts result in counts from 0 to 255 (full scale); thus each count represents a phase difference of 648 nsec/256 = 2.53 nsec. This is the resolution of the system, i.e., the minimum detectable phase difference.

Every 8192 cycles of the reference clock, i.e., approximately every 5.308 msec (a rate of 188.4 Hz), the software simultaneously samples the coarse (differential counters) and fine (A/D output) phase detectors and combines their readings into a composite total representing integer and fractional values of a unit interval. This total retains the 2.53 nsec resolution described above.



NOTE:

Resolution is NOT the same as accuracy. Accuracy is defined as the maximum allowable fractional frequency offset.

From the phase data, the processor calculates TIE, MTIE, and slip (193 bit slip) over an observation interval selected through the 5405 card. Jitter is calculated over a one-second interval, using a 10 Hz high pass filter. The clock recovery circuit used for jitter measurements acts as a single pole low pass filter for jitter frequencies above 23 kHz. TIE and MTIE are calculated using a 10 Hz low pass filter.

TIE, MTIE, slip, and jitter information is sent to the 5405 Information Management Card for storage and later reporting and, if certain thresholds are exceeded (refer to Table 4-A), the corresponding front panel yellow LED is turned on. If commanded by the 5405 card, raw phase measurements are accumulated over the observation interval for later reporting.

5.725 Model 5404, 8-bit Analog/Digital Converter

The 8-bit A/D converter converts fine phase information from analog to digital for processing by the microprocessor.

5.726 Microprocessor

The 5404 is a microprocessor-controlled monitoring system which measures DS1 error and performance parameters of up to five DS1 inputs. One of the five inputs is selected either manually by the front panel MON SELECT button or by automatic scan at user-controlled intervals through the 5405 card. The selected input number appears on the seven segment display and its signal is passed to a clock and data recovery circuit.

The microprocessor, data latch, address decoder, random access memory (RAM), and read only memory (ROM) perform all the controlling and communication functions of the card.

5.727 Bit Slip between A and B Clocks

Independent of other measurements, the bit slip between the A and B clocks is determined and displayed alternately with the number of the input being monitored. A rotating display shows every 1/4 bit slip. An excessive slip rate triggers a major alarm.

5.728 Clock Select

Clock select chooses Clock A, Clock B, Input A, or Input B as reference for the phase detector.

5.729 Controls and Indicators

The 5404 generates autonomous alarm reports via the 5405 card when selected thresholds are exceeded or when the A/B clock slip exceeds one bit in 30 minutes (major alarm).

The following controls and indicators appear on the front panel of the card. A number of the yellow indicators, in any combination, may be on at the same time. LED data buffers provide latches and drivers for the various LED indicators:

a. The red FUSE LED lights if the on-card fuse blows.

b. The yellow LOS LED indicates loss of signal or loss of sync.

c. The yellow OOF LED indicates out of frame.

(continued)

5.729 (continued)

d. The yellow BPV LED indicates excessive bipolar violations rate.

e. The yellow CRC6 LED indicates excessive code errors.

f. The yellow TIE LED indicates excessive time interval error.

g. The yellow MTIE LED indicates excessive maximum time interval error.

h. The yellow SLIP LED indicates one frame slip.

i. The yellow JITTER LED indicates excessive jitter.

j. The seven segment display (SCAN) briefly shows the new input being monitored when the input is changed; otherwise the display shows bit slip between the two clock cards.

k. The MON SELECT pushbutton is used for manually selecting one of the five DS1 inputs. In the SCAN state, a single push of the button advances the 5404 card to the next available input. In the manual mode, a double push returns the 5404 to the SCAN state.

l. The red A/B SLIP LED indicates A/B clock bit slip.

5.7210 Input Jack

The MON IN jack allows the fifth DS1 input signal to be received via front panel access.

5.7211 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt, 100 mA battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.7212 DC-to-DC Converter

The DC-to-DC converter converts –48 Vdc battery input to +5 Vdc to operate all active devices on the card.

5.8 Model 5405 Information Management Card

5.801 This card provides microprocessor-controlled communications within the STS 5400 system and with the outside world. The 5402, 5403, 5410, and 5412 clock cards communicate with the 5405 Information Management Card, along with the 5404 Synchronization Monitor Card, to provide an interface to an operation support system (OSS). The 5405 polls the clocks and the 5404 card and retrieves operational status, collected data, and alarm information. It also sets the modes of the clocks for maintenance purposes and controls the data gathering modes on the 5404.

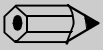
5.802 The 5405 Information Management Card is provisioned at the factory in the following configurations:

a. Model 5405-4 supports the AA input architecture and provides a TL1 interface.

b. Model 5405-5 supports the AA input architecture and provides a Menu interface.

c. Model 5405-8 supports the AB input architecture and provides a TL1 interface.

d. Model 5405-9 supports the AB input architecture and provides a Menu interface.



NOTE:

The 5405 version must support the same input architecture, AA or AB, as the track and hold cards. See Appendix A.

NOTE:

Refer to the TL1 User Manual, Larus Practice 80-802-193, for Transaction Language 1 instructions. Refer to the Menu User Manual, Larus Practice 80-801-193, for Menu instructions.

5.81 Functions

5.811 The Model 5405 Information Management Card provides:

a. Local and remote status reporting.

b. Performance reporting.

c. Alarm reporting through two RS-232 ports to remote access or a local type craft terminal, operating at 1200 to 9600 baud asynchronous.

d. An RS-232 port for remote access by an operations system which can be configured to interface a packet assembler/disassembler (PAD) connecting to an X.25 packet network.

e. Message format either on menu screens or in the TL1 language.

5.82 Circuit Description

The 5405 block diagram appears in Figure 5-7.

5.821 Alarm Interface Data Latch

The 5405 receives alarm signals from every other card in the shelf and processes these to report alarm status (refer to 5406, Alarm Interface Card, below).

5.822 Microprocessor

The microprocessor, data latch, address decoder, RAM, and ROM perform all the controlling and communication functions of this card.

5.823 Asynchronous Communication Serial Controller

A serial communication controller connects to two RS-232 ports on the backplane, one for a local asynchronous terminal and the other for a remote terminal or operating system via an asynchronous modem or X.25 PAD. Depending on the programmable read only memory (PROM) installed, the message format can be either menu screens, defined in Larus Practice 80-801-193, or a TL1 message set, defined in Larus Practice 80-802-193.

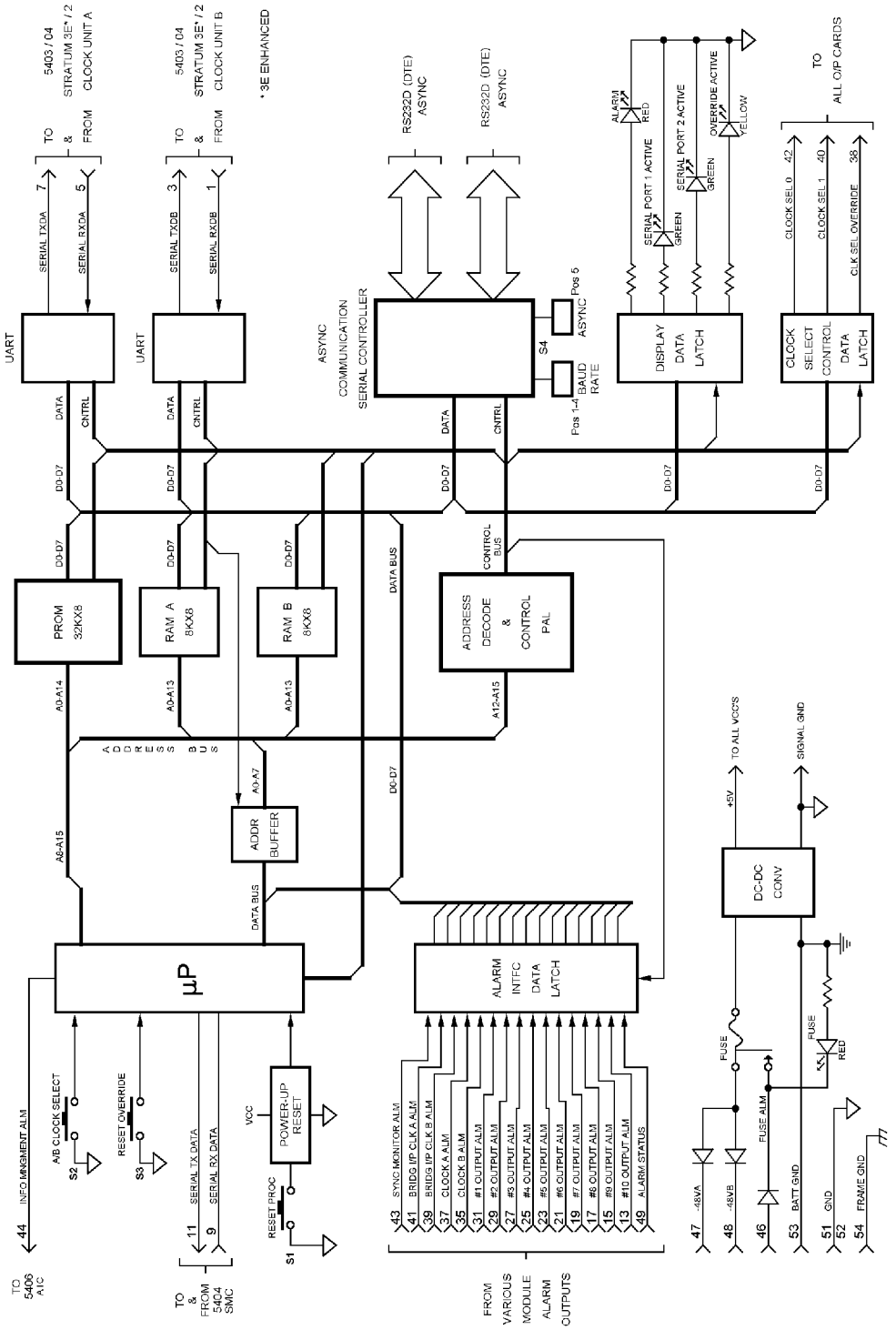


Figure 5-7. Model 5405 Information Management Card

5.824 UARTs and Buffer

Two universal asynchronous receiver/transmitters provide serial data links to the A and B clock cards for status reporting and clock mode control. A serial port built into the processor exchanges data and commands with the 5404 Synchronization Monitor Card.

5.825 RAM A/B

Random access memory of 16 kbytes on the card provides storage of alarm and performance data obtained from the 5404 card. Half the RAM is volatile and half is nonvolatile.

5.826 Clock Select Data Latch

Three lines extending to the output cards allow for control of clock selection.

5.827 Display Data Latch

LED data buffers provide latches and drivers for the various LED indicators.

5.828 Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED lights if the on-card fuse blows.

b. The green PORT 1 LED lights when serial port 1 is active.

c. The green PORT 2 LED lights when serial port 2 is active.

d. The yellow OVERRIDE LED lights when manual override for clock selection is active.

e. The red ALARM LED lights when an alarm condition exists.

f. The RESET PROC pushbutton resets the processor.

g. The RESET O/R pushbutton allows for manual override of clock selection.

h. The A/B CLOCK SELECT pushbutton allows for selection of Clock A, Clock B, Input A, or Input B.

5.829 Model 5405, Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.8210 DC-to-DC Converter

The DC-to-DC converter converts –48 Vdc battery input to +5 Vdc to operate all active devices on the card.

5.9 Model 5406 Alarm Interface Card

5.901 The STS 5400 system allows for one Alarm Interface Card. This card receives alarm information from all the other cards.

5.91 Functions

5.911 The Model 5406 Alarm Interface Card performs the following functions:

a. Collects alarm status information from all cards in the system.

b. Determines whether the overall alarm state is Major or Minor.

c. Provides floating relay contact closures for Major and Minor, audible and visual summary alarms.

d. Sends detailed alarm information to the 5405 Information Management Card.

5.92 Circuit Description

The 5406 block diagram appears in Figure 5-8.

5.921 Alarm Interface Logic

This card collects alarm information from every other card in the shelf, determines whether any combination of alarms creates a Major or Minor alarm state, and activates the alarm relays and corresponding Major or Minor LED indicators.

a. Minor alarms include:

Any single card failure.
Any combination of failures that leaves at least one clock in its tracking mode and at least one set of outputs available from even/odd pairs of output cards, e.g. OUT 1 (slot J8) and OUT 2 (slot J9).

(continued)

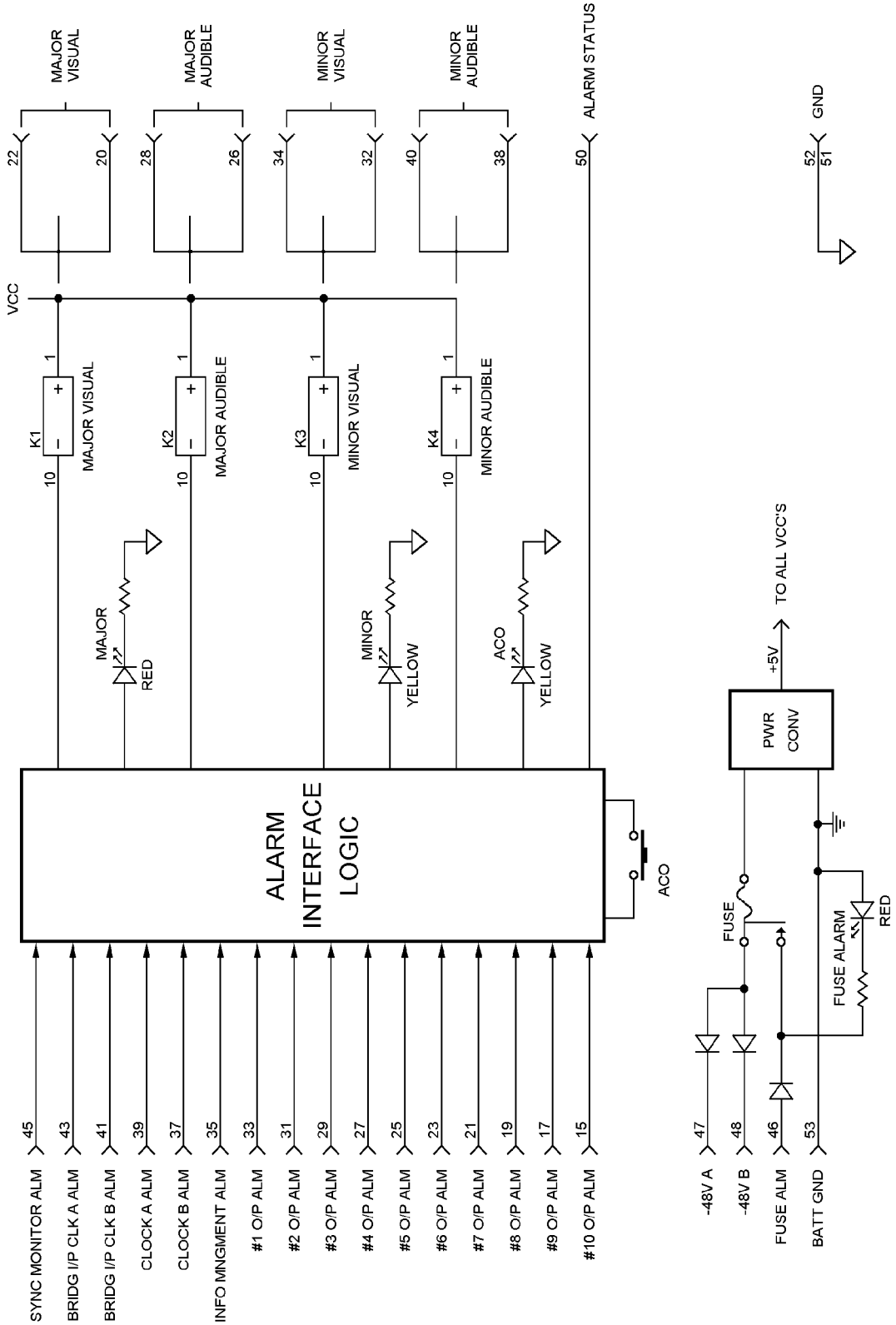


Figure 5-8. Model 5406 Alarm Interface Card

5.921 (continued)

b. Major alarms result from:

Both input cards A and B invalid.
Clock A and Clock B not tracking.
Two or more output cards (even and odd) in alarm.
Bit slip between A and B clocks reported by the Synchronization Monitor Card.

5.922 Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED lights if the on-card fuse blows.

b. The red MAJOR LED indicates a Major alarm condition.

c. The yellow MINOR LED indicates a Minor alarm condition.

d. The alarm cutoff (ACO) pushbutton shuts off the audible alarms and lights the yellow ACO LED. If another alarm comes on, the audible alarm is once more activated. When the alarm condition clears, all alarms are reset and the ACO LED goes out.

5.923 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.10 Model 5407 DS1 Output Driver Card

5.1001 This card provides ten separate DS1 DSX-compatible framed ones drive signals, with either SF or ESF framing. The signals drive any standard DS1 receiver through up to 655 feet of cable. An alarm output signal alerts the 5406 Alarm Interface Card when one or more outputs have failed.

5.101 Functions

5.1011 The Model 5407 DS1 Output Driver Card provides the following:

a. Clock selection by a logic array based on HOLD indications from the A and B track and hold cards. The current tracking card or, if both are in HOLD, the last track and hold card to go into the HOLD state is selected. Switching is nonrevertive to minimize the number of phase disturbances.

(continued)

5.1011 (continued)

b. Override lines from the 5405 Information Management Card allowing for manual clock selection and for automatic switching directly to a reference input in the event that both track and hold cards fail (Major alarm state).

c. The first output card from the left (any slot) acting as a master selector and all other output cards slaved to it, to ensure that all output cards select the same clock reference.

d. A synchronization bus connecting all output cards to ensure that all outputs from the shelf are frame and multiframe synchronized for DS1 SF (12 frame multiframe), DS1 ESF (24 frame multiframe), and E1 (16 frame multiframe) outputs.

e. On-card switch selection of SF or ESF framing.

5.102 Circuit Description

The 5407 block diagram appears in Figure 5-9.

5.1021 Clock Select Switch

The clock select switch is a 1.544 MHz clock selector with phase buildout circuit, frame/byte synchronization system, LED indicators, and output alarms. The selector output goes to a phase buildout circuit whose function is to smooth out sudden phase changes (which might be as much as ±1/2 a unit interval) occurring when the clock selection is changed. The change of phase rate is limited to under 20 nanoseconds (1/32 unit interval) in 14 milliseconds (21,616 unit intervals).

5.1022 DS1 Transmit Framer

The DS1 transmit framer is clocked by the signal selected by the clock select switch. The signal is frame synchronized with the buffered signal from the external synchronization bus. It inserts either SF or ESF framing according to the setting of S1, and produces dual rail output pulses that the output drivers convert to bipolar framed all ones.

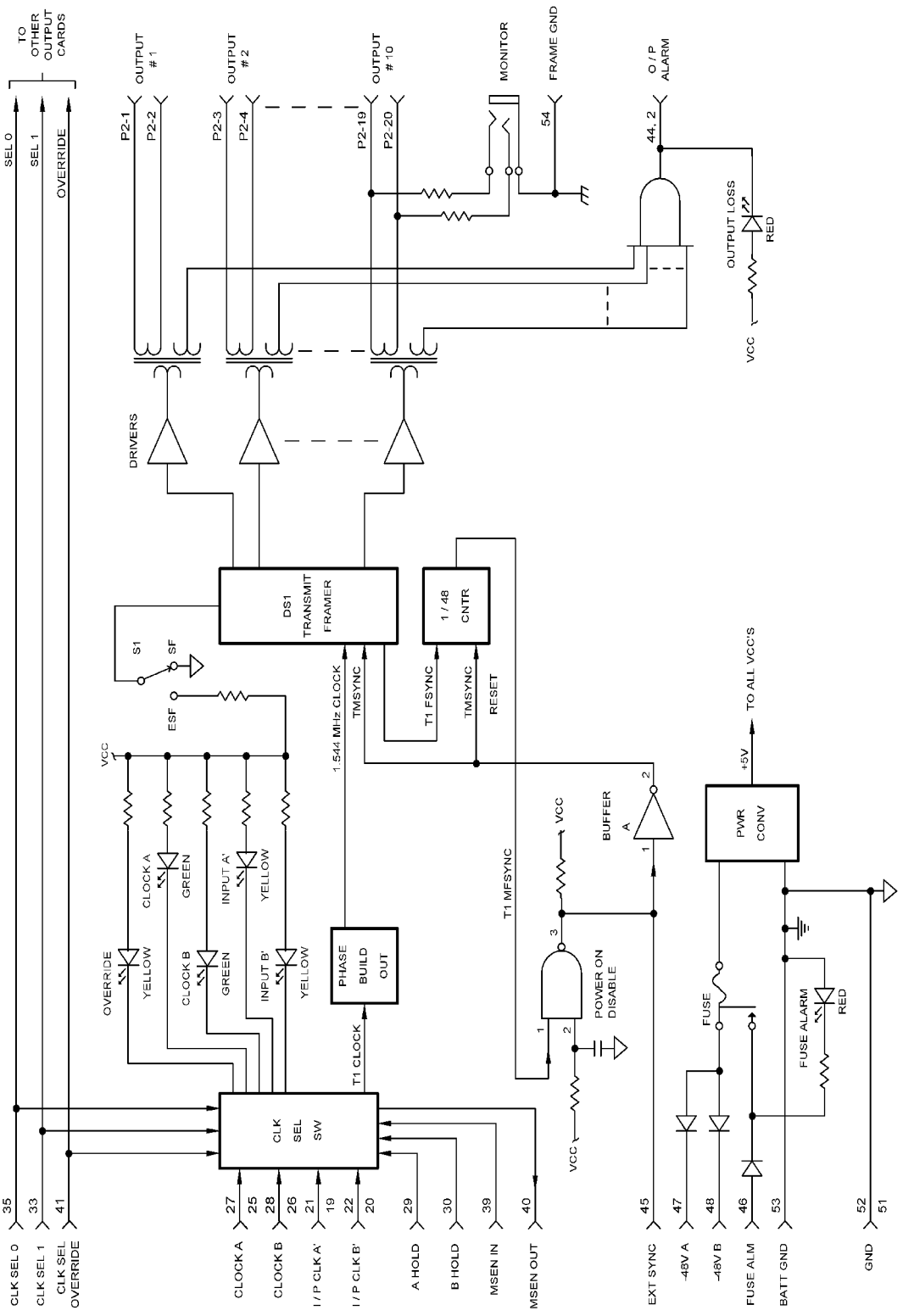


Figure 5-9. Model 5407 DS1 Output Driver Card

5.1023 Model 5407, Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED lights if the on-card fuse blows.

b. The green CLOCK A/B LED lights when the corresponding clock, either A or B, is selected.

c. The yellow INPUT A/B LED lights when the corresponding input, either A or B, is selected.

d. The yellow OVERRIDE LED lights when automatic selection has been overridden by manual remote selection.

e. The red OUTPUT LOSS LED lights when a loss of one or more outputs occurs. If both A and B clocks and both input references fail, leaving no valid signal for the output cards to select, the OUTPUT LOSS LEDs on all output cards are illuminated and all outputs are suppressed.

f. The front panel MON jack allows for monitoring one of the output signals with a standard monitoring test set. The Model 5407 has ten outputs with independent drivers.

5.1024 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.11 Model 5408 Composite Clock Output Driver Card

5.1101 This 64 kbps card provides ten separate composite clock outputs for driving D4 channel banks and other equipment that require composite clock inputs. One or more failed outputs activate an alarm.

5.111 Functions

5.1111 The Model 5408 Composite Clock Output Driver Card provides the following:

a. Ten separate composite clock drive signals.

b. An alarm output bus that alerts the 5406 Alarm Interface Card when one or more outputs have failed.

5.1111 (continued)

NOTE:

All outputs must be terminated in 130 ohms for the output failure alarm to operate properly.

c. Clock selection by a logic array based on HOLD indications from the A and B clock cards. The current tracking clock or, if both are in HOLD, the last clock to go into the HOLD state is selected. Switching is nonrevertive to minimize the number of phase disturbances.

d. Override lines from the 5405 Information Management Card allowing for manual clock selection and for automatic switching directly to a reference input in the event that both clocks fail (Major alarm state).

e. The first output card from the left (any slot) acting as a master selector and all other output cards slaved to it to ensure that all output cards select the same clock reference.

f. A synchronization bus connecting all output cards to ensure that all outputs from the shelf are frame and multiframe synchronized for DS1 SF (12 frame multiframe), DS1 ESF (24 frame multiframe), and E1 (16 frame multiframe) outputs. All composite clock outputs are byte synchronized.

5.112 Circuit Description

The 5408 block diagram appears in Figure 5-10.

5.1121 Clock Select Switch

The clock select switch is a 1.544 MHz clock selector with phase buildout circuit, byte synchronization system, LED indicators, and output alarms. The selector output goes to a phase buildout circuit whose function is to smooth out sudden phase changes (which might be as much as ±1/2 a unit interval) occurring when the clock selection is changed.

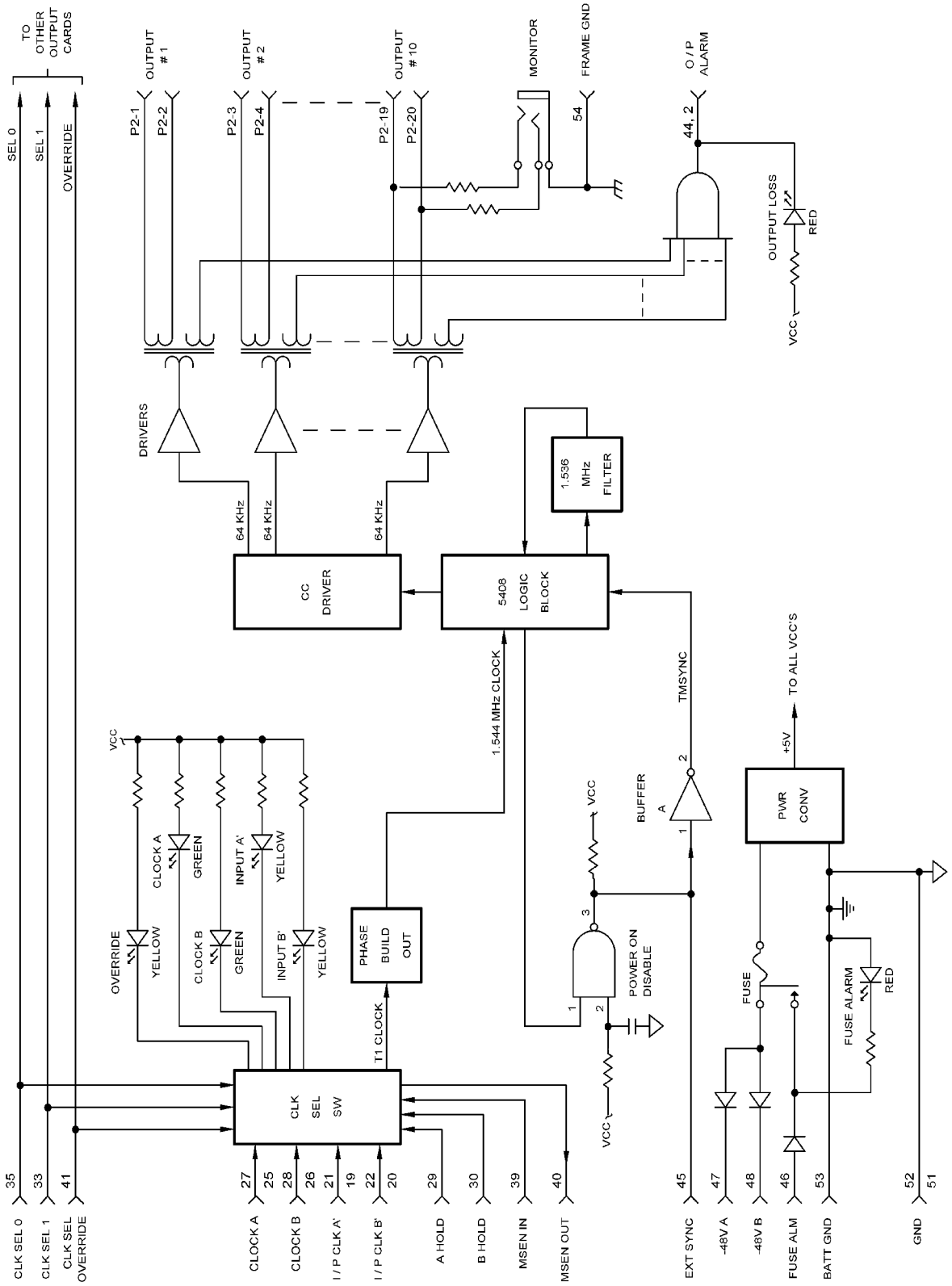


Figure 5-10. Model 5408 Composite Clock Output Driver Card

5.1122 Model 5408, Logic Block

The 5408 logic block is clocked by the selected clock signal and frame synchronized from the external synchronization bus. It produces 1.536 MHz which is filtered externally from the clock output. The 1.536 MHz is divided by .24 to produce the 64 kHz composite clock (CC). The logic block also contains a circuit which disables the drivers if no input clock is present.

The block also produces synchronizing pulses which synchronize the 8 kHz BPVs in the composite clock signals. The CC drive provides bipolar signals to the output drivers.

The power-on disable provides time delay to ensure the card is disabled until the power supply stabilizes after power is applied.

5.1123 Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED lights if the on-card fuse blows.

b. The green CLOCK A/B LED lights when the corresponding clock, either A or B, is selected.

c. The yellow INPUT A/B LED lights when the corresponding input, either A or B, is selected.

d. The yellow OVERRIDE LED lights when automatic selection has been overridden by manual remote selection.

e. The red OUTPUT LOSS LED lights when a loss of one or more outputs occurs. If both A and B clocks and both input references fail, leaving no valid signal for the output cards to select, the OUTPUT LOSS LEDs on all output cards are illuminated and all outputs are suppressed.

f. The front panel MON jack allows for monitoring one of the output signals with a standard monitoring test set. The Model 5408 has ten outputs with independent drivers.

5.1124 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.12 Model 5409 E1 Output Driver Card

5.1201 The 5409 List 2 E1 Output Driver Card provides ten separate outputs of E1 (nominally 2.048 Mbps) framed ones. The 5409 List 3 provides ten outputs of 2.048 MHz square wave signals. The 5409 List 4 is the same as List 2 with the addition of CAS and CRC4 multiframe synchronization configuration switches. Each output will drive a 120 ohm load through up to 200 meters of 22 AWG cable. One or more failed outputs will activate an alarm.

5.121 Functions

5.1211 The Model 5409 E1 Output Driver Card provides the following:

a. E1 clock, either E1 compatible framed ones (Lists 2 and 4) or 2.048 MHz square wave signals (List 3).

b. An alarm output bus that alerts the 5406 Alarm Interface Card when one or more outputs have failed.

c. Clock selection by a logic array based on HOLD indications from the A and B clock cards. The current tracking clock or, if both are in HOLD, the last clock to go into the HOLD state is selected. Switching is nonrevertive to minimize the number of phase disturbances.

d. Override lines from the 5405 Information Management Card allowing for manual clock selection and for automatic switching directly to a reference input in the event that both clocks fail (Major alarm state).

e. The first output card from the left (any slot) acting as a master selector and all other output cards slaved to it to ensure that all output cards select the same clock.

f. A synchronization bus connecting all output cards to ensure that all outputs from the shelf are frame and multiframe synchronized for DS1 SF (12 frame multiframe), DS1 ESF (24 frame multiframe), and E1 (16 frame multiframe) outputs.

g. On the 5409 List 4 only, CAS and CRC4 multiframe synchronization configuration switches.

5.122 Circuit Description

The 5409 block diagram for Lists 2 and 3 appears in Figure 5-11, the block diagram for List 4 in Figure 5-12.

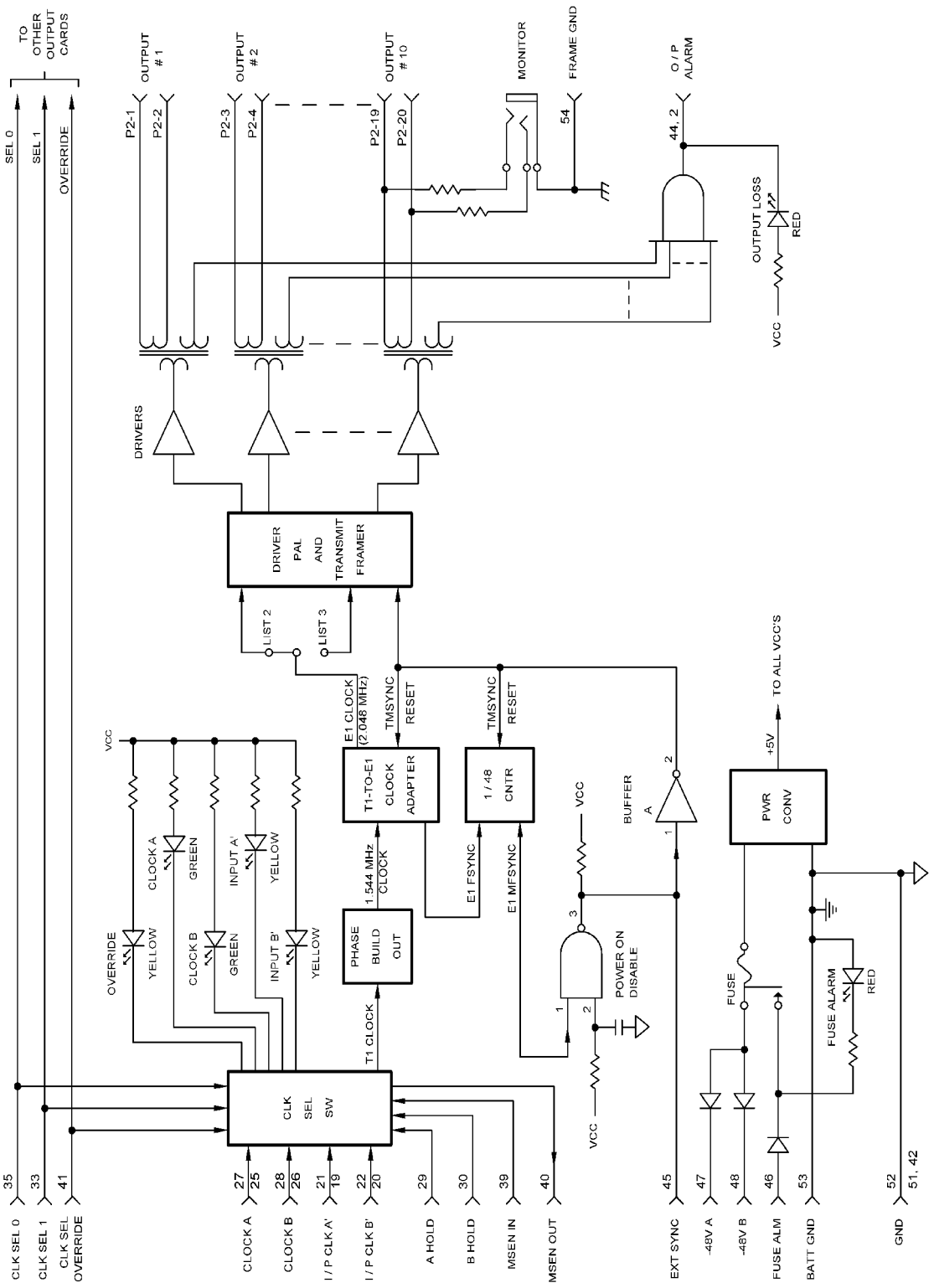


Figure 5-11. Model 5409 2/ 3 E1 Output Driver Card

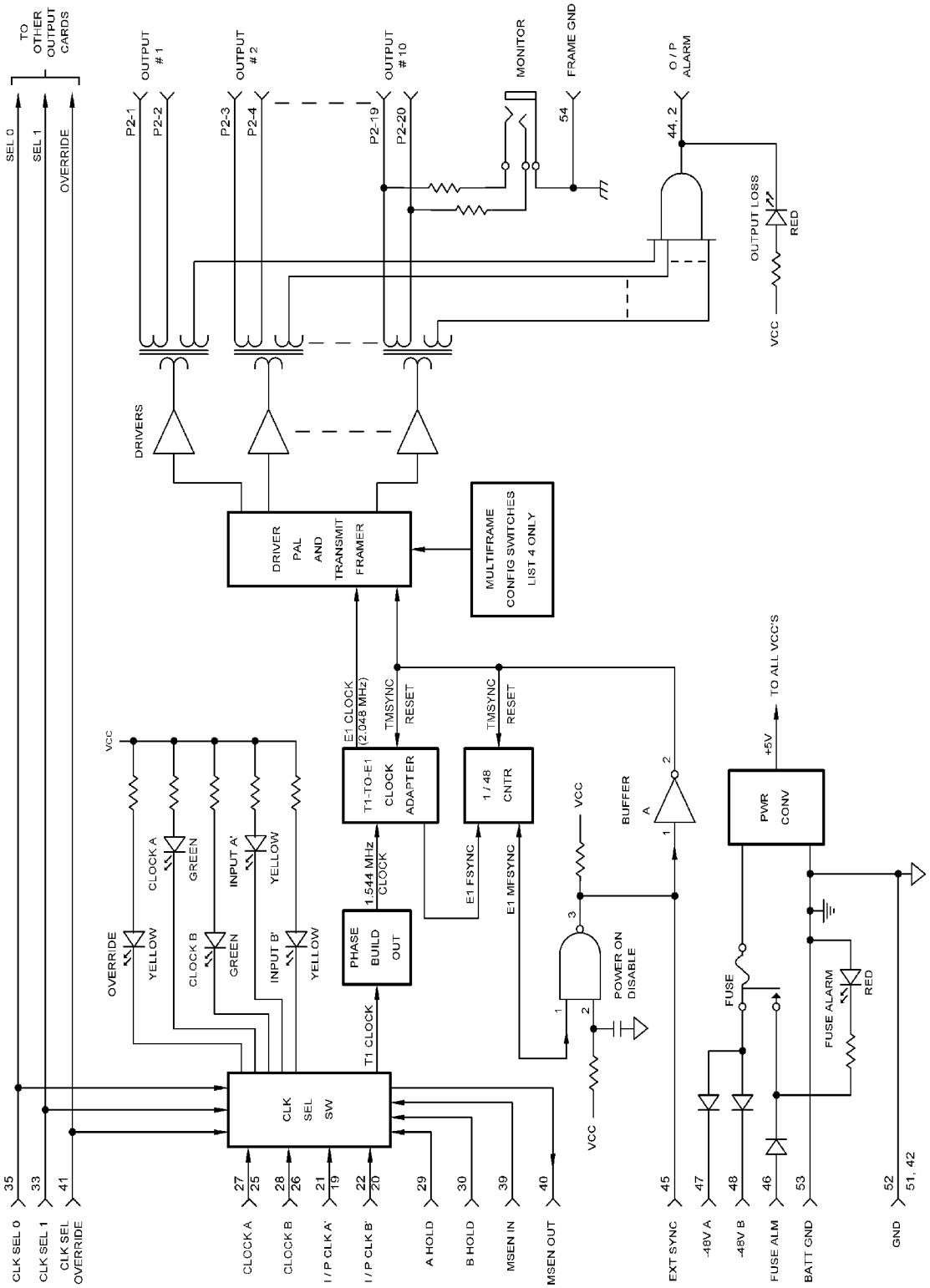


Figure 5-12. Model 5409-4 E1 Output Driver Card

5.1221 Model 5409, Clock Select Switch

The clock select switch is a 1.544 MHz clock selector with phase buildout circuit, frame/byte synchronization system, LED indicators, and output alarms. The selector output goes to a phase buildout circuit whose function is to smooth out sudden phase changes (which might be as much as ±1/2 a unit interval) occurring when the clock selection is changed. The change of phase rate is limited to under 81 nanoseconds in 1.326 milliseconds.

5.1222 Clock Adapter

A clock adapter chip produces a 2.048 MHz clock which is phase locked to the 1.544 MHz clock selected at the input. The 5409 List 3 card converts the clock adapter output to a square wave and feeds it to the output drivers.

5.1223 E1 Transmit Framer

The 5409 List 2 and List 4 cards are equipped with an E1 transmit framer, clocked by the clock adapter output and frame synchronized from the external synchronization bus. It inserts E1 framing words and produces dual rail output pulses which the output drivers convert to bipolar framed all ones.

5.1224 Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED lights if the on-card fuse blows.

b. The green CLOCK A/B LED lights when the corresponding clock, either A or B, is selected.

c. The yellow INPUT A/B LED lights when the corresponding input, either A or B, is selected.

d. The yellow OVERRIDE LED lights when automatic selection has been overridden by manual remote selection.

e. The red OUTPUT LOSS LED lights when a loss of one or more outputs occurs. If both A and B clocks and both input references fail, leaving no valid signal for the output cards to select, the OUTPUT LOSS LEDs on all output cards are illuminated and all outputs are suppressed.

f. The front panel MON jack allows for monitoring one of the output signals with a standard monitoring test set. The Model 5409 cards have ten outputs with independent drivers.

5.1225 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.13 Model 5410 GPS Stratum 1 Track and Stratum 2 Hold Card

5.1301 There are one or two 5410 cards in the Stratum 1/2 system. The standard GPS antenna unit is supplied with the 5410 card. Antenna mounting guidelines are contained in the Installation manual, Larus Practice 80-600-193.

5.1302 The 5410 is provisioned at the factory as follows:

Model 5410-2 supports the AB input architecture.
The AA input architecture is not supported.

NOTE:

Both track and hold cards in a system must support the same input architecture, in this case AB. See Appendix A.

5.131 Functions

5.1311 The Model 5410 GPS Stratum 1 Track and Stratum 2 Hold Card performs the following functions:

a. Accepts one GPS reference signal and provides timing and a smoothed signal to the output cards from a rubidium oscillator tracking a GPS signal. The card also accepts one of two optional 1.544 MHz DS1 signals for a tracking reference if the GPS receiver should fail. Refer to Figure 5-13 for a flow chart tracking the 'health' of the GPS module.

(continued)

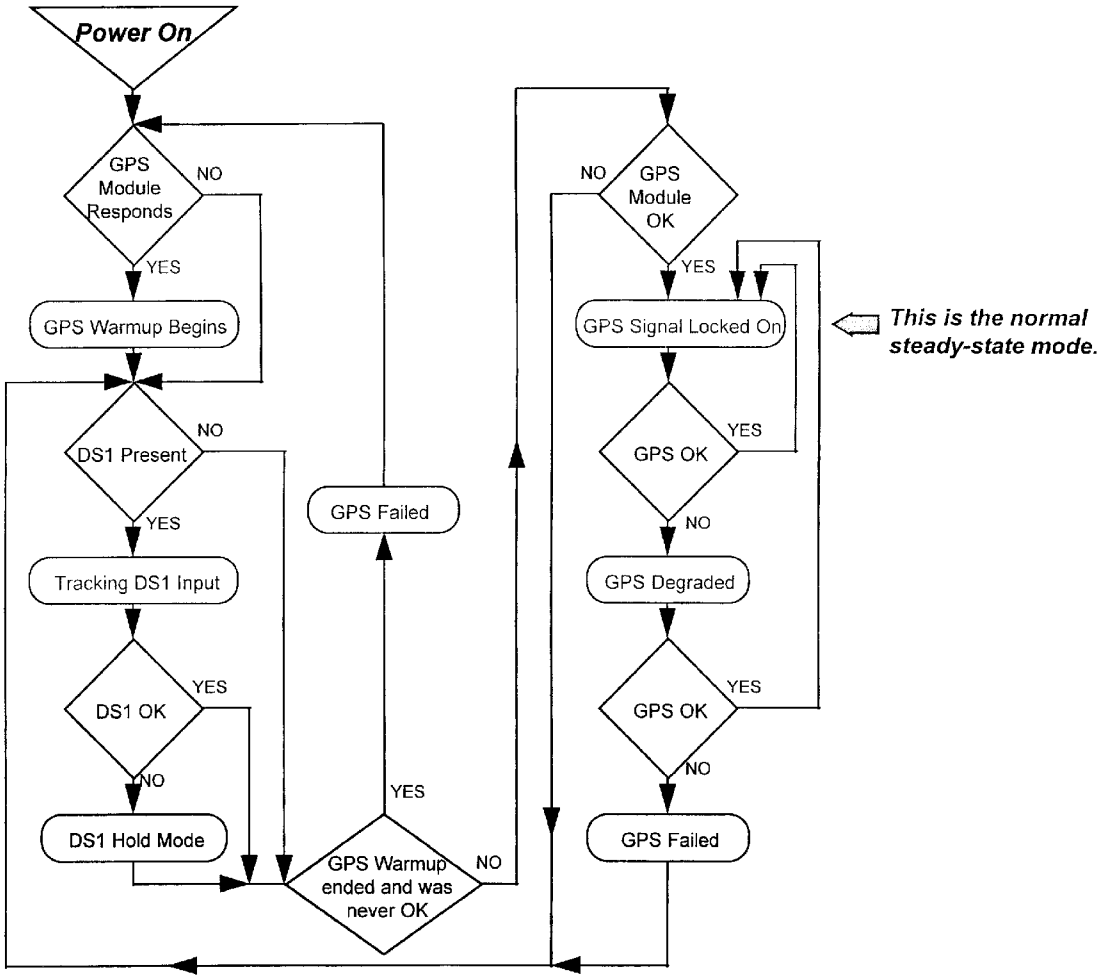


Figure 5-13. Model 5410/5412 Card GPS Mode Algorithm

5.1311 Model 5410, Functions (continued):

b. If the GPS receiver fails, monitors the DS1 reference input for framing, CRC6, and out-of-specification errors. If a sustained input error occurs, the 5410 will hold to the last known reference with a drift of less than 7.5×10^{-11} in 24 hours. The signal to the output cards is continuous (no phase hits) during any switch from track to hold. Frequency and phase corrections occur over periods of about 10,000 seconds. A fast ACQUIRE state reduces this to 300 seconds for power-up and 1000 seconds for return from the HOLD state.

c. Accepts an alternate external 10 MHz signal from a high stability timing source such as a GPS receiver, cesium clock, or similar mechanism. This signal may be used to replace the 10 MHz reference from the on-board precision oscillator or as a tracking input. The external 10 MHz signal is selected as a reference by on-card switches/jumpers. It is selected as a tracking reference through user commands to the 5405 Information Management Card.

d. Supplies monitoring and alarm information to the 5405 and 5406 cards.

5.132 Circuit Description

Refer to the 5410 block diagram in Figure 5-14 in the following discussion.

5.1321 Inputs

a. GPS Receiver

The 5410 card supplies the GPS receiver with the 10 MHz rubidium oscillator reference. The receiver determines the error in the 10 MHz with respect to the GPS signal. The microprocessor reads the error from the GPS receiver and sends a correction to the DDFS setting.

b. DS1 Input

The 5410 card has its own DS1 input circuits and does not require a separate input card. It selects either the A or B input via the analog switch. For the AB architecture, the A card selects the A input and the B card selects the B input. (The AA architecture is not supported.) The selection is automatic; it can be changed manually from a terminal connected to the 5405 Information Management Card.

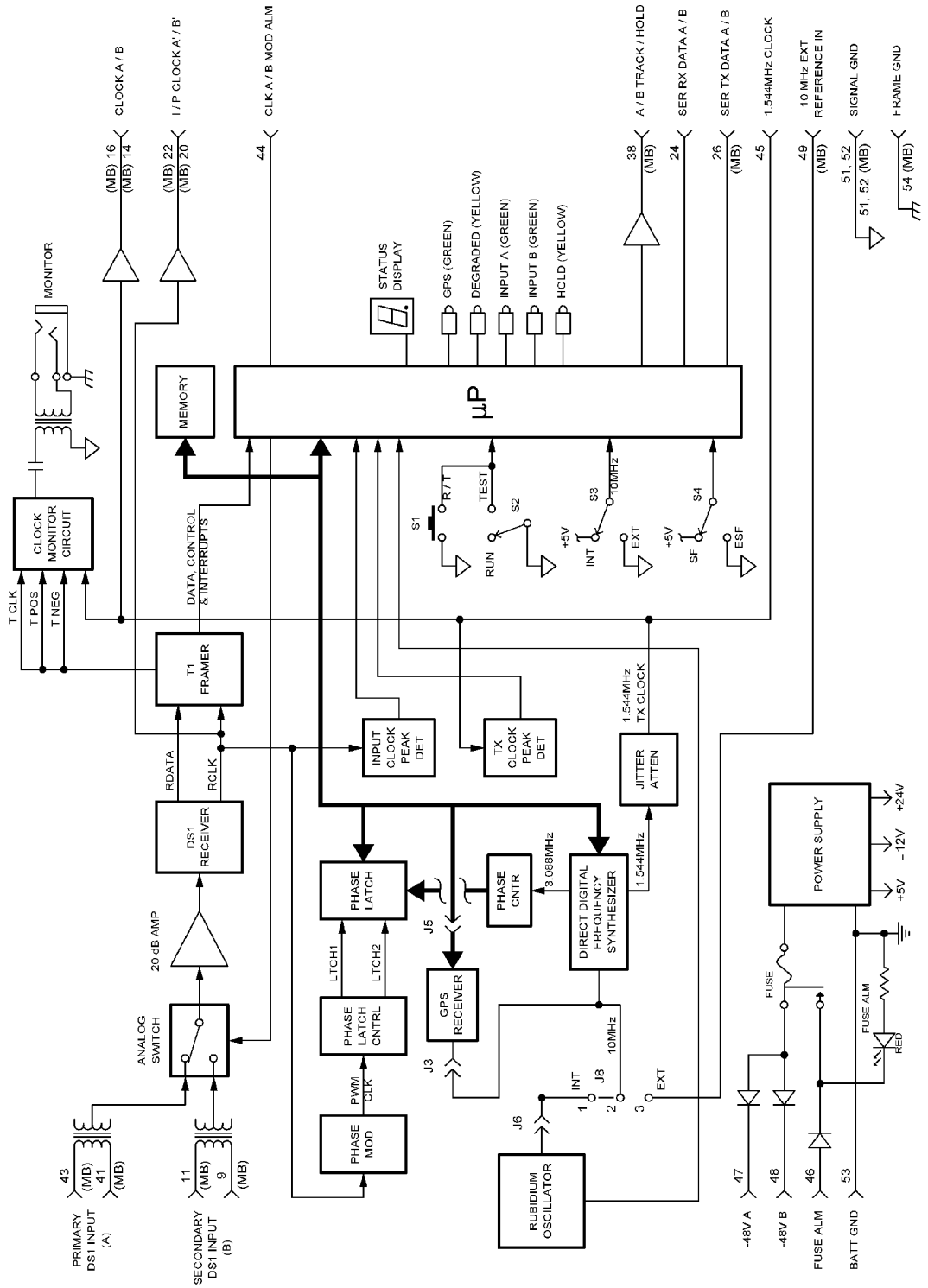


Figure 5-14. Model 5410 GPS Stratum 1 Track and Stratum 2 Hold Card

5.1322 DS1 Receiver

The DS1 receiver regenerates the selected incoming signal and recovers both the clock and the data. The data go to the framing circuit.

5.1323 Framer

The framing circuit detects the following framing errors:

a. Yellow Alarm, LOS (175 ±75 consecutive zeros)

b. BPVs

c. Invalid CRC6 codes (ESF framing only)

An impaired signal causes the microcontroller to cease tracking, go into the HOLD mode, and show the type of impairment on the seven segment display.

5.1324 Rubidium Oscillator

A 10 MHz rubidium oscillator provides the input reference to the GPS receiver and the 48-bit DDFS.

5.1325 Direct Digital Frequency Synthesizer

The oscillator is coupled to the DDFS and acts as a reference for it. The DDFS operates on the presumption that oscillator frequency is kept within a reasonable degree of precision, e.g. within one part in 10^{+9}. The DDFS uses a digital process to convert the oscillator signal into a signal having a second related frequency. The DDFS accomplishes this conversion by utilizing a stored algorithm and a numerical input from the microprocessor.

The DDFS accepts an integer, N, from the microprocessor. The synthesizer then generates a new output frequency 'F out' from 'F osc' according to the following formula:

$$F\ out = \frac{(N)\ (F\ osc)}{2^{48}}$$

where 48 is the number of bits used by the DDFS and (F osc) is nominally 10 MHz.

5.1326 Model 5410, Controls and Latches

The output phase is compared with the phase of the recovered input reference clock by means of a pair of counters and latches, good signal or bad:

a. When the input signal is deemed good, the microcontroller tracks the input phase and, every 7 seconds, calculates a new 48-bit control word for the DDFS based on the input/output phase difference and rate of change. The 24 MSBs of the control word are fixed and the microcontroller calculates the 24 LSBs.

b. When the input is deemed bad, tracking ceases (HOLD mode). Any fault which triggers the HOLD state saves the last known good output frequency correction factor and uses it to determine the HOLD frequency.

5.1327 Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED indicates an internal fuse has blown.

b. The green GPS LED indicates sufficient timing information has been received for a valid GPS mode.

c. The yellow DEGRADED LED indicates GPS timing has been lost and Stratum 1 mode is still in effect, however degraded in performance.

d. The green INPUT A/B LEDs indicate which of the two input signals the card is tracking.

e. The yellow HOLD LED indicates that the unit is in the HOLD mode.

f. The green LEDs plus the yellow LED glowing simultaneously indicate that the card is in alarm (Invalid Output).

g. The seven segment display indicates the STATUS of the output failure.

h. The TEST pushbutton causes the microcontroller to execute a diagnostic routine and display 'H' if successful. The unit returns to normal tracking in a few seconds. (This function only operates if the unit is tracking DS1 signals, not in the GPS mode.)

5.1328 Model 5410, Alarm Output

The HOLD or INVALID OUTPUT condition, or a fault reported by the rubidium oscillator, results in a card alarm output to the 5406 Alarm Interface Card and to the 5405 Information Management Card. A data link to the 5405 card allows the 5410 card to report its status (tracking, hold, stand-alone, or failed).

5.1329 Clocks A and B

Each of the two 5410 cards in a normal redundant system drives a Clock A or B differential 1.544 MHz bus to the ten output card slots. Each card also drives a hold indicator bus. Selection of the A or B clock is done by logic circuitry on the output cards.

5.13210 External 10 MHz Signal

The external 10 MHz signal input is intended for an external reference oscillator in place of the 'ON CARD' oscillator. Such a signal could come from a cesium clock, a GPS or LORAN C receiver, or similar source.

The external 10 MHz signal may be selected as the reference to the DDFS in place of the on-board 10 MHz precision oscillator by the appropriate setting of on-board switches/jumpers. When the external 10 MHz signal is selected for this purpose, a period ('.') will appear on the seven segment display.

If the external 10 MHz reference is selected and is not present, the track and hold card will not provide an output to its clock bus but will go into the alarm state. The front panel INPUT A, INPUT B, and HOLD LEDs will light simultaneously. If there is no other track and hold card in the system, the output driver card(s) will select one of the two DS1 inputs to output. If, under this condition, the DS1 input is not present or fails, a false signal will be present at the output. This signal will be delivered to the output driver card(s) and will appear on the system outputs. This is NOT a valid signal. The system will be indicating multiple failures and sending notifications from the 5405 Information Management Card to user terminals.

The external 10 MHz signal may also be selected as a tracking input in place of the DS1 inputs. Selection is done by TL1 or Menu user commands through the interfaces of the 5405 Information Management Card.

5.13210 Model 5410, External 10 MHz Signal (continued)

If the external 10 MHz signal is selected as a tracking input and is not present, the track and hold card will go into holdover mode and light the HOLD LED on its front panel. The output driver cards will switch to use the signal from the other track and hold card, if present, or one of the two DS1 inputs.

NOTE:

It is possible to select the external 10 MHz Signal as both an external reference and a tracking input at the same time but this is not a valid mode of operation.

5.13211 Monitor Jack

A front panel DS1 monitor jack (–20 dB referenced to the DSX-1) provides framed all ones at the clock output frequency.

5.13212 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

5.14 Model 5412 GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card

5.1401 The Model 5412 is comprised of a 5402 Stratum 3E Enhanced Track and Hold Card with a GPS receiver to provide Stratum 1 performance. There are one or two 5412 cards in the Stratum 1/3E system. The standard GPS antenna unit is supplied with the 5412 card.

5.1402 The 5412 is provisioned at the factory as follows:

Model 5412-2 supports the AB input architecture.
The AA input architecture is not supported.

NOTE:

Both track and hold cards in a system must support the same input architecture, in this case AB. See Appendix A.

5.141 Functions

5.1411 The Model 5412 GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card performs the following functions:

a. Accepts one GPS reference signal and provides timing and a smoothed signal to the output cards from an ovenized crystal oscillator tracking a GPS signal. The card also accepts one of two optional 1.544 MHz DS1 signals for a tracking reference if the GPS receiver should fail. Refer to Figure 5-13 for a flow chart tracking the 'health' of the GPS module.

b. If the GPS receiver fails, monitors the DS1 reference signal for framing, CRC6, and out-of-specification errors. If there is an input error, the unit holds the last known reference with a drift of less than 5×10^{-9} in 24 hours. The signal to the output cards is continuous (no phase hits) during any switch from track to hold. Frequency and phase corrections occur over periods of about 3000 seconds. A fast ACQUIRE state reduces this to 100 seconds for power-up and 300 seconds for return from the HOLD state.

c. Accepts an alternate external 10 MHz signal from a high stability timing source such as a GPS receiver, cesium clock, or similar mechanism. This signal may be used to replace the 10 MHz referencefrom the on-board precision oscillator or as a tracking input. The external 10 MHz signal is selected as a reference by on-card switches/jumpers. It is selected as a tracking reference through user commands to the 5405 Information Management Card.

d. Supplies monitoring and alarm information to the 5405 and 5406 cards.

5.142 Circuit Description

Refer to the 5412 block diagram in Figure 5-15 in the following discussion.

5.1421 Inputs

a. GPS Receiver

The 5412 card supplies the GPS receiver with the 10 MHz crystal oscillator reference. The receiver determines the error in the 10 MHz with respect to the GPS signal. The microprocessor reads the error from the GPS receiver and provides a correction to the DDFS setting.

(continued)

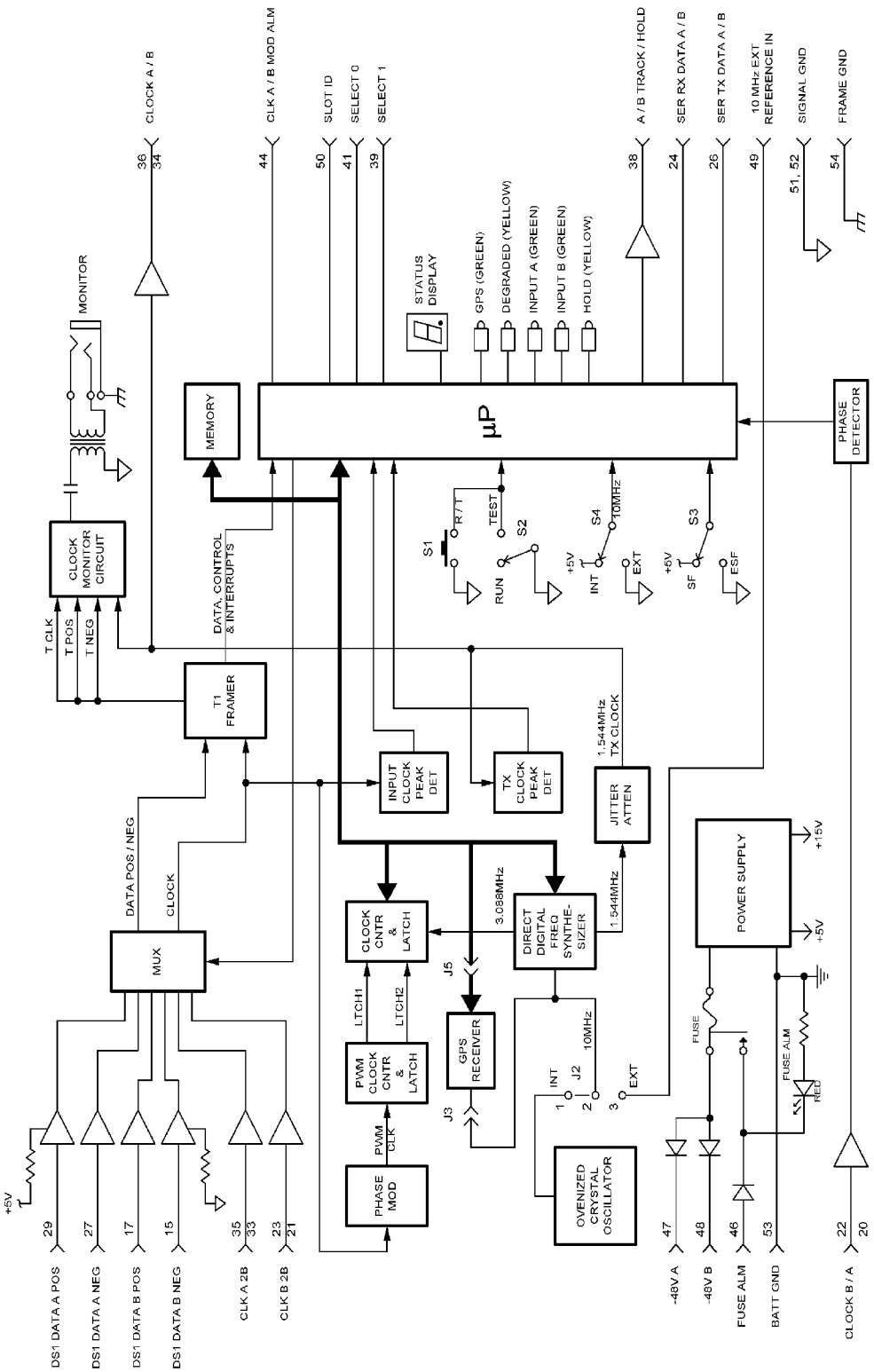


Figure 5-15. Model 5412 GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card

5.1421 (continued)

b. DS1 Input

The 5412 card receives its inputs from its corresponding 5401 Input Card. It selects either the A or B input via the analog switch. A given 5412 becomes the A clock or B clock depending on the shelf slot in which the card is installed. For the AB architecture, the A card selects the A input and the B card selects the B input. (The AA architecture is not supported.) The selection is automatic; it can be changed manually from a terminal connected to the 5405 Information Management Card.

5.1422 DS1 Receiver

The DS1 receiver regenerates the selected input signal and recovers both the clock and the data. The data go to the framing circuit. The 5412 compares the DS1 reference bit time phase relative to the ovenized crystal oscillator reference using a digital phase detector. Samples of phase information are collected and averaged, over about a one-second period, to provide input to the control algorithm to update the frequency synthesizer. If, at any point in the accumulation and calculation period, an excessive error condition (LOS, LOF, etc.) is detected which causes the collected information to be suspect, the unit enters the holdover state and does not update the frequency synthesizer. If the data are qualified, then the update will proceed. After 128 acquire cycles (about 2 minutes) following initial input qualification, the track and hold card will be in the tracking mode. After 5 to 7 minutes, the tracking mode will be at minimum error if the input is within specifications. The 5412 will track timing signals from any other Stratum 3 or better source (that is, Stratum 2 or 1) having a frequency offset of no more than ± 7.1 Hz.

5.1423 Framer

The framing circuit detects the following framing errors:

a. Yellow Alarm, LOS (175 ± 75 consecutive zeros)

b. BPVs

c. Invalid CRC6 codes (ESF framing only)

An impaired signal causes the microcontroller to cease tracking, go into the HOLD mode, and show the type of impairment on the seven segment STATUS display.

5.1424 Ovenized Crystal Oscillator

A 10 MHz ovenized crystal oscillator provides the input to a 48-bit DDFS.

5.1425 Model 5412, Direct Digital Frequency Synthesizer

The oscillator is coupled to the DDFS and acts as a reference for it. The DDFS operates with the presumption that oscillator frequency is kept within a reasonable degree of precision, e.g. within one part in 10^8. The DDFS uses a digital process to convert the oscillator signal to a signal having a second related frequency. The DDFS accomplishes this conversion by utilizing a stored algorithm and a numerical input from the microprocessor.

The DDFS accepts an integer, N, from the microprocessor. The synthesizer then generates a new output frequency 'F out' from 'F osc' according to the following formula:

$$F\ out = \frac{(N)\ (F\ osc)}{2^{48}}$$

where 48 is the number of bits used by the DDFS and (F osc) is nominally 10 MHz.

5.1426 Controls and Latches

The output phase is compared with the phase of the recovered input reference clock by means of a pair of counters and latches, good signal or bad:

a. When the input signal is deemed good, the microcontroller tracks the input phase and, every 7 seconds, calculates a new 48-bit control word for the DDFS based on the input/output phase difference and rate of change. The 24 MSBs of the control word are fixed and the microcontroller calculates the 24 LSBs.

b. When the input is deemed bad, tracking ceases (HOLD mode). Any fault which triggers the HOLD state saves the last known good output frequency correction factor and uses it to determine the HOLD frequency.

5.1427 Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED indicates an internal fuse has blown.

b. The green GPS LED indicates sufficient timing information has been received for a valid GPS mode.

c. The yellow DEGRADED LED indicates GPS timing has been lost and Stratum 1 mode is still in effect, however degraded in performance.

d. The green INPUT A/B LEDs indicate which of the two input signals the card is tracking.

e. The yellow HOLD LED indicates that the unit is in the HOLD mode.

f. The green LEDs plus the yellow LED glowing simultaneously indicate that the card is in alarm (Invalid Output).

g. The seven segment STATUS display indicates the reason for the output failure.

h. The TEST pushbutton causes the microcontroller to execute a diagnostic routine and display 'H' if successful. The unit returns to normal tracking in a few seconds. (This function only operates if the unit is tracking DS1 signals, not in the GPS mode.)

5.1428 Alarm Output

The HOLD or INVALID OUTPUT condition results in a card alarm output to the 5406 Alarm Interface Card and the 5405 Information Management Card. A data link to the 5405 card allows the 5412 card to report its status (tracking, hold, stand-alone, or failed).

5.1429 Clocks A and B

Each of the two 5412 cards in a normal redundant system drives a clock A or B differential 1.544 MHz bus to the ten output card slots. Each card also drives a hold indicator bus. Selection of the A or B clock is done by logic circuitry on the output cards.

5.14210 External 10 MHz Signal

The external 10 MHz signal input is intended for an external reference oscillator in place of the 'ON CARD' oscillator. Such a signal could come from a cesium clock, a GPS or LORAN C receiver, or similar source.

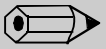
The external 10 MHz signal may be selected as the reference to the DDFS in place of the on-board 10 MHz precision oscillator by the appropriate setting of on-board switches/jumpers. When the external 10 MHz signal is selected for this purpose, a period ('.') will appear on the seven segment display.

5.14210 Model 5412, External 10 MHz Signal (continued)

If the external 10 MHZ reference is selected and is not present, the track and hold card will not provide an output to its clock bus but will go into the alarm state. The front panel INPUT A, INPUT B, and HOLD LEDs will light simultaneously. If there is no other track and hold card in the system, the output driver card(s) will select one of the two DS1 inputs to output. If, under this condition, the DS1 input is not present or fails, a false signal will be present at the output. This signal will be delivered tothe output driver card(s) and will appear on the system outputs. This is NOT a valid signal. The system will be indicating multiple failures and sending notifications from the 5405 Information Management Card to user terminals.

The external 10 MHz signal may also be selected as a tracking input in place of the DS1 inputs. Selection is done by TL1 or Menu User commands through the interfaces of the 5405 Information Management Card.

If the external 10 MHz signal is selected as a tracking input and is not present, the track and hold card will go into holdover mode and light the HOLD LED on its front panel. The output driver cards will switch to use the signal from the other track and hold card, if present, or one of the two DS1 inputs.



NOTE:

It is possible to select the external 10 MHz Signal as both an external reference and a tracking input at the same time but this is not a valid mode of operation.

5.14211 Monitor Jack

A front panel DS1 monitor jack (–20 dB referenced to the DSX-1) provides framed all ones at the clock output frequency.

5.14212 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

NOTE:

Refer to subsection 5.6 for clock operation, substituting Model 5412 for 5402 and Model 5410 for 5403 in the text.

5.15 Model 5413 EIA RS-422 Output Driver Card

5.1501 This card provides ten separate EIA RS-422 compatible differential square wave outputs. The outputs drive any standard RS-422 compatible receiver through up to 400 feet of cable. An alarm output signal alerts the 5406 Alarm Interface Card when one or more outputs have failed.

5.1502 The 5413 card is provisioned at the factory in one of two configurations:

Model 5413-0 has an output frequency of 1.544 MHz.
Model 5413-1 has an output frequency of 8 kHz.

5.151 Functions

5.1511 The Model 5413 EIA RS-422 Output Driver Card provides the following:

a. Clock selection based on HOLD indications from the A and B track and hold cards. The current tracking card or, if both are in HOLD, the last track and hold card to go into the hold state is selected. Switching is nonrevertive to minimize the number of phase disturbances.

b. Override lines from the 5405 Information Management Card allowing for manual clock selection and for automatic switching directly to a reference input in the event that both clocks fail (Major alarm state).

c. The first output card from the left (any slot) acting as a master selector and all other output cards slaved to it to ensure that all output cards select the same clock reference.

d. A synchronization bus connecting all output cards to ensure that all outputs from the shelf are synchronized.

5.152 Circuit Description

The 5413 block diagram appears in Figure 5-16.

5.1521 Clock Select Switch

The clock select switch is a 1.544 MHz clock selector with phase buildout circuit, LED driver, and output alarm controller. The selector output goes to a phase buildout circuit whose function is to smooth out sudden phase changes (which might be as much as ±1/2 a unit interval) when the clock selection is changed. The change of phase rate is limited to under 20 nanoseconds (1/32 unit interval) in 14 milliseconds (21,616 unit intervals).

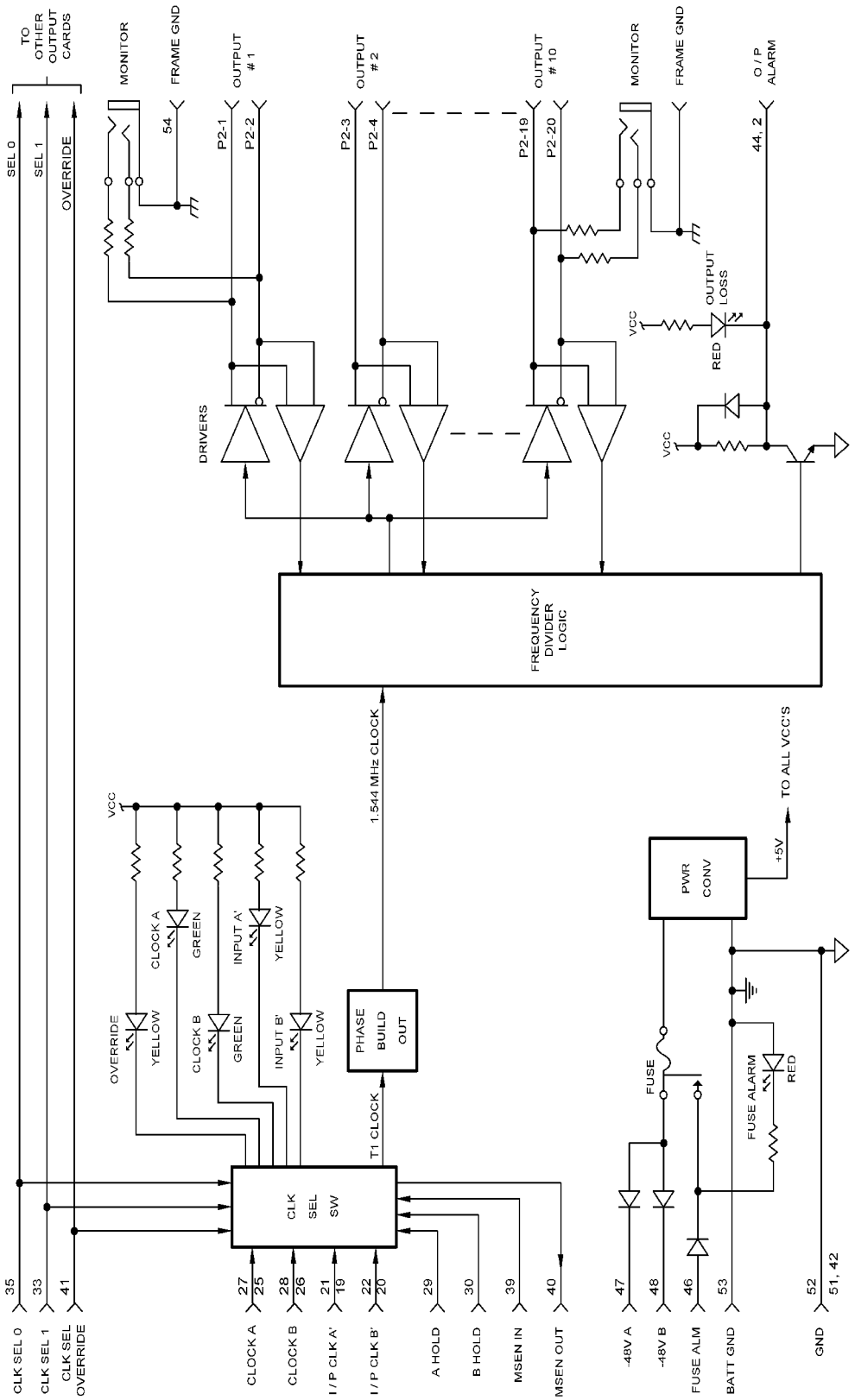


Figure 5-16. Model 5413 EIA RS-422 Output Driver Card

5.1522 Model 5413, Logic Block

The logic block provides a frequency divider circuit that offers an output that is rationally related to the input frequency.

5.1523 Controls and Indicators

The following controls and indicators appear on the front panel of the card:

a. The red FUSE LED lights if the on-card fuse blows.

b. The green CLOCK A/B LED lights when the corresponding clock, either A or B, is selected.

c. The yellow INPUT A/B LED lights when the corresponding input, either A or B, is selected.

d. The yellow OVERRIDE LED lights when automatic selection has been overridden by manual remote selection.

e. The red OUTPUT LOSS LED lights when a loss of one or more outputs occurs. If both A and B clocks and both input references fail, leaving no valid signal for the output cards to select, the OUTPUT LOSS LEDs on all output cards are illuminated and all outputs are suppressed.

f. The front panel MON jack allows for monitoring one of the output signals with a standard monitoring test set. The Model 5413 has ten outputs with independent drivers.

5.1524 Power

An on-card power converter provides the necessary circuit voltages from the diode-combined A and B –48 volt battery supplies. The on-card fuse, if it blows, lights the red FUSE LED and provides battery to the Fuse Alarm bus connecting to pin 10 on the backplane terminal strip TB1.

Warranty 6

6.01 Products Manufactured by Larus Corporation

Limited Warranty:

a. Larus products, except as stated otherwise in an applicable price list, are warranted against defects in workmanship and material for a period of 1 (one) year from date of delivery as evidenced by Larus' packing slip or other transportation receipt. Warranty under contract may differ. Components in Larus products manufactured by others shall be assigned the original manufacturer's warranty. Refer to paragraph 6.03.

b. Larus' sole responsibility under this warranty shall be either to repair or replace, at its option, any component which fails during the applicable warranty period because of a defect in workmanship and material, provided purchaser has promptly reported same to Larus in writing. All replaced products or parts shall become Larus' property.

c. Larus will only honor the warranty at its repair facility in San Jose, California, unless stipulated differently under contract. It is the purchaser's responsibility to return, at its expense, the allegedly defective product to Larus. The purchaser must obtain a return merchandise authorization (RMA) number and shipping instructions from Larus prior to returning any product under warranty. Transportation charges for the return of the product to the purchaser shall be paid by Larus within the United States. For all other locations, the warranty excludes all costs of shipping, customs clearance, and other related charges. If Larus determines that the product is not defective within the terms of this warranty, the purchaser shall pay Larus all costs of handling, transportation, and repairs at the then prevailing repair rates.

d. All the above warranties are contingent upon proper use of the product. These warranties will not apply (i) if adjustment, repair, or parts replacement is required because of accident, unusual physical, electrical, or electromagnetic stress, neglect, misuse, failure of electric power, environmental controls, transportation, not maintained in accordance with Larus specifications, or abuses other than ordinary use; (ii) if the product has been modified by the purchaser or has been repaired or altered outside Larus' factory, unless Larus specifically authorizes such repairs or alterations; (iii) where Larus serial numbers, warranty data, or quality assurance decals have been removed or

altered.

6.01 (continued)

e. Larus also reserves the right to make product improvements without incurring any obligation or liability to make the same changes in products previously manufactured or purchased. In no event shall Larus be liable for any breach of warranty in an amount exceeding the net selling price of any defective product. No person, including any dealer, agent, or representative of Larus, is authorized to assume for Larus any other liability on its behalf except as set forth herein. Non-payment of any invoice rendered within the stated payment terms automatically cancels any warranty or guarantee stated or implied. If any payment is due Larus for services performed hereunder, it shall be subject to the same payment terms as the original purchase.

f. Except for the express warranties stated herein, Larus disclaims all warranties on products furnished hereunder, including, without limitation, all implied warranties of merchantability and fitness, and the stated express warranties are in lieu of all obligations or liabilities on the part of Larus arising out of or in connection with the performance of the products.

6.02 Repaired Products and Repair Parts

Products repaired within the warranty period continue to be warranted to the end of that period or for 90 (ninety) days, whichever is longer. Repair work done on products repaired outside the warranty period is warranted against defects in workmanship and material for a period of 90 (ninety) days.

6.03 Products and Components Manufactured by Others

For products or components not manufactured by Larus, the original manufacturer's warranty shall be assigned to the purchaser to the extent permitted and is in lieu of any other warranty, expressed or implied. For warranty information on a specific product, a written request should be made to Larus.

NOTE: Features and specifications are subject to change without notice.

Equipment Issue Information 7

7.01 Practice 80-100-193, Issue 5, applies to the following equipment:

Description	Model Number	Equipment Issue
19/23 Inch Rack Mounting Shelf without GPS capability, Stratum 2 Silkscreen	5400, List 3	1
19/23 Inch Rack Mounting Shelf without GPS capability, Stratum 3E Silkscreen	5400, List 3A	1
19/23 Inch Rack Mounting Shelf with GPS capability	5400, List 4	3
DS1 Bridging Input Card	5401, List 1	1
Stratum 3E Enhanced Track and Hold Card	5402, List 3 (AB) 5402, List 4 (AA)	3 3
Stratum 2 Track and Hold Card	5403, List 3 (AB) 5403, List 4 (AA)	3 4
Synchronization Monitor Card	5404, List 3	4
Information Management Card:		
TL1 Language	5405, List 4 (AA)	5
Menu Screens	5405, List 5 (AA)	3
TL1 Language	5405, List 8 (AB)	1
Menu Screens	5405, List 9 (AB)	1
Alarm Interface Card	5406, List 0	4
DS1 Output Driver Card, 10 outputs	5407, List 2	6
Composite Clock Output Driver Card, 10 outputs	5408, List 1	3

(continued)

7.01 (continued)

Description	Model Number	Equipment Issue
E1 Output Driver Card, 10 outputs	5409, List 2	1
2.048 MHz Square Wave Output Driver Card, 10 outputs	5409, List 3	1
E1 Output Driver Card with multiframe synchronization configuration switches, 10 outputs	5409, List 4	1
GPS Stratum 1 Track and Stratum 2 Hold Card	5410, List 2 (AB)	1
GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card	5412, List 2 (AB)	1
EIA RS-422 Output Driver Card, 10 Outputs	5413, List 0 (1.544 MHz)	3
	5413, List 1 (8 kHz)	3

Appendix A

STS 5400 AA vs. AB Architecture

1. A redundant STS 5400 system contains two input track and hold assemblies. A single assembly is one of the following:

   - One 5401 DS1 Bridging Input Card plus
     One 5402 Stratum 3E Enhanced Track and Hold Card (AA or AB) or
     One 5412 GPS Stratum 1 Track and Stratum 3E Enhanced Hold Card (AB)
     OR
   - One 5403 Stratum 2 Track and Hold Card (AA or AB)
     OR
   - One 5410 GPS Stratum 1 Track and Stratum 2 Hold Card (AB)

   NOTE:

   In a system that includes the Model 5405 Information Management Card, the 5405 and track and hold card versions must support the same input architecture, AA or AB.

2. There are one to ten output driver cards in the system. Each card is capable of switching between timing reference signals from DS1 Input 1, DS1 Input 2, Input Track and Hold A, and Input Track and Hold B. The first input track and hold assembly to power up and produce timing pulses will be the active timing source for the output driver cards.

3. Assuming there is no operator intervention:

   Systems with AA architecture (refer to Figure AA-1) have both input track and hold assemblies tracking the same input, DS1 Input 1 or DS1 Input 2. If there is a failure of the tracked input, both assemblies go into holdover mode and search between DS1 Input 1 and DS1 Input 2 for a good input. Each assembly will independently acquire and track the first valid input signal that becomes available after entering the holdover mode.

   Systems with AB architecture (Figure AA-2) have each input track and hold assembly tracking a different input, i.e., Input Track and Hold A tracking DS1 Input 1, Input Track and Hold B tracking DS1 Input 2, or vice versa. If there is a failure of the primary input, the active input track and hold assembly goes into holdover mode and switches to track the secondary input.

(continued)

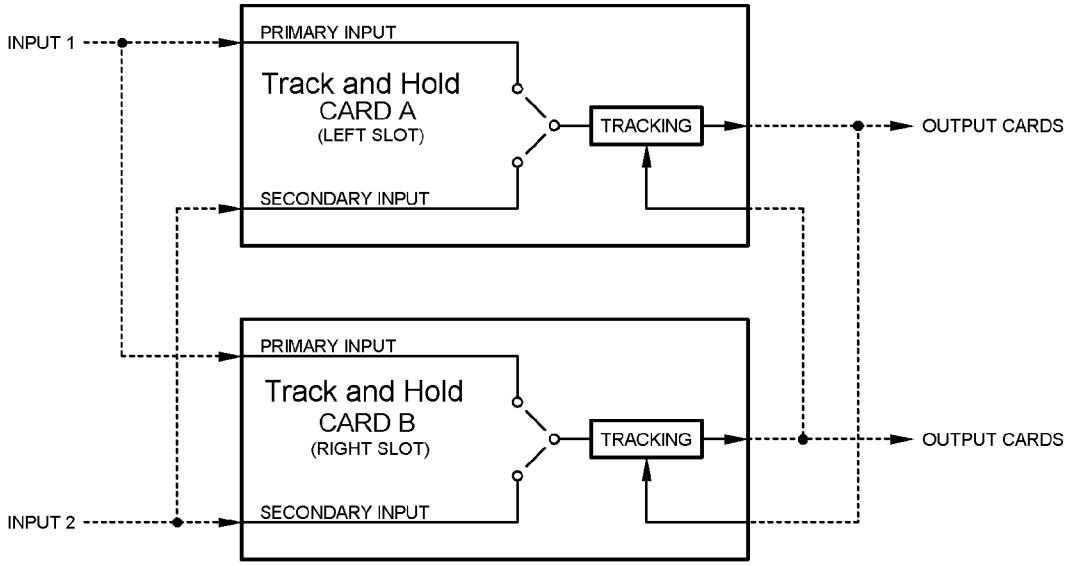


Figure AA-1. Model STS 5400 AA Clock Architecture

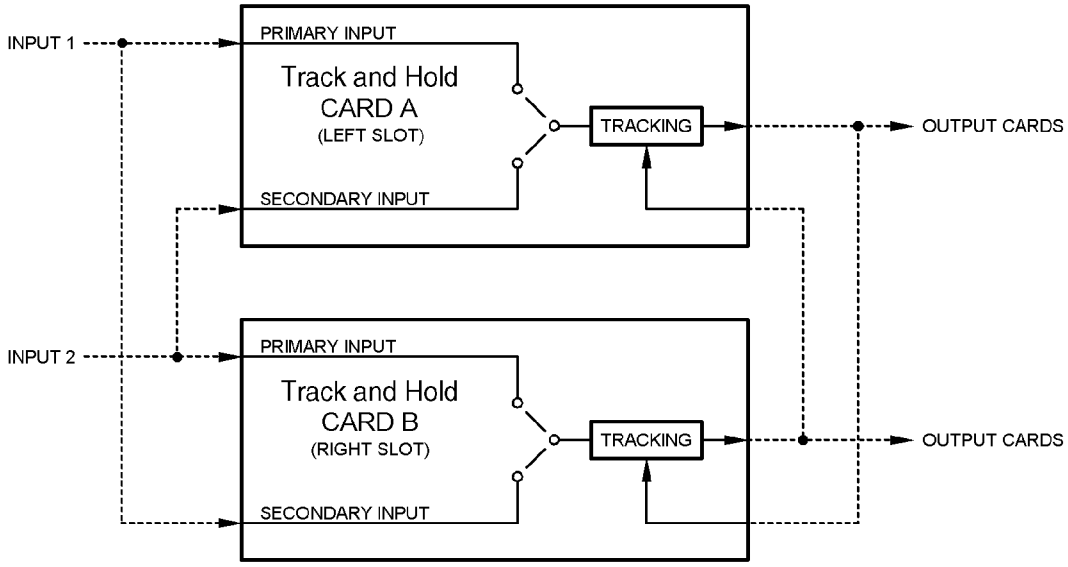


Figure AA-2. Model STS 5400 AB Clock Architecture

3. (continued)

   Whichever the architecture, the system is nonrevertive. For example, in an AB system architecture, Input Track and Hold A is tracking DS1 Input 1 as its primary input and is the active source being used by the output cards. If there is a failure of DS1 Input 1, Input Track and Hold A will go into holdover mode and check whether the secondary input is good. If it is, Input Track and Hold A will switch to track the secondary input. Subsequently, if the primary input returns and is good, the Input Track and Hold A will not switch back to tracking the primary signal unless the secondary input fails.

   In either case, the better input track and hold assembly will drive the output driver cards. If the active assembly stops the output of timing pulses or goes into holdover mode, the output driver cards will switch to use the other assembly as a timing reference. If both input track and hold assemblies cease to produce pulses, the output driver cards will switch to use either DS1 Input 1 or DS1 Input 2 as a timing reference.

4. In both architectures, during normal operation:

   - Each track and hold card monitors either its primary or secondary input. Under most circumstances, both cards will monitor the same type of input (primary or secondary).

   - The track and hold card selected for output tracks its monitored input.

   - The track and hold card not selected for output tracks the output of the other track and hold card (if the other card is selected for output).

   - If its currently monitored input is no longer good, a track and hold card will switch to monitoring its other input (primary or secondary).

   - If both primary and secondary inputs are no longer good, the track and hold card will go into a HOLD state.

   - If at least one of the inputs becomes good, the track and hold card will exit the HOLD state. If both inputs become good within 10 seconds, the primary input will be monitored.

[This page is intentionally left blank.]

Appendix B

STS 5400 System Behavior: Phase Alignment

1. A redundant STS 5400 system contains two track and hold cards. The output of one is used by the output driver cards and is referred to as the primary track and hold. The other card is in reserve and is called the secondary track and hold. If there is a failure of the primary track and hold card, it signals the output cards so that they switch to use the output from the secondary card.

2. The two track and hold cards are crossconnected via the backplane to allow each track and hold to monitor the other one. The phase alignment feature causes the secondary card to continually attempt to align its phase with the primary card. The relative phase alignment is updated approximately once every 8 seconds. This means that the secondary track and hold changes its phase very slowly as it tries to align its output with the primary track and hold. The phase alignment process may take many seconds initially, depending on the relative phase between the input references being tracked by each card. Once aligned, the secondary card's output phase should remain within a few nanoseconds of the primary card's output.

3. The phase alignment feature minimizes the jump in phase in the system outputs when the output driver cards switch between the two track and hold references. The 5407, 5409, and 5413 output driver cards contain circuitry to limit the output phase change rate to a maximum of 20 nanoseconds in 14 milliseconds.

[This page is intentionally left blank.]

Glossary

TRACK AND HOLD CARDS -- DEFINITION OF TERMS

A. Clock Performance

1. Accuracy

   Fractional frequency offset of the oscillator in the free running or stand-alone state, over a specified time and temperature range, compared with the ideal frequency. Offset is determined by the oscillator module's initial calibration, aging, and temperature performance, as specified by the manufacturer.

2. Acquisition Time

   a. Time interval from power-up to the time at which normal tracking is achieved (refer to item 6 below). For a cold start, there will be an additional warmup time of several minutes to allow the oscillator to approach operating temperature. After warmup, the clock enters the ACQUIRE 1 state for a specified time, as indicated on the clock state diagram (Figure 3-3). This is a relatively fast tracking state so the initial clock frequency offset (see item 8 below) is quickly reduced to near zero, then the clock enters ACQUIRE 2. After the settling time (refer to item 9), normal tracking is achieved.

   b. When the oscillator has been in holdover, the time interval from when a good reference signal reappears to the time at which normal tracking is achieved (refer to item 6). From holdover, the clock enters the ACQUIRE 2 state for a specified time (Figure 3-3). This is an intermediate tracking state, in which any frequency offset that has accumulated in holdover is reduced more quickly than it would be in the normal tracking mode.

3. Free Run, Stand-alone

   Operating states in which the oscillator has never been locked to an external reference since power-up and the software has set the frequency to a predetermined nominally correct value. The free running state is entered from power-up if no external reference is present. The stand-alone state is entered if the RUN/TEST switch on the board is in the TEST position.

4. Holdover

   Operating state in which the oscillator is not locked to an external reference but is using data acquired during previous tracking to maintain its accuracy, with respect to the last known comparison, with a synchronization reference.

5. Holdover Drift, Holdover Stability

   Fractional frequency change (Δ f)/f occurring over a specified time interval and temperature range when the oscillator is in the holdover state. This change depends on the oscillator's aging and temperature characteristics and on the accuracy of tracking at the time holdover was entered.

6. Normal Tracking

   State that exists when the clock oscillator is locked to an external synchronization reference. Tracking performance is equal to or better than the maximum time interval error (MTIE) mask specified in Figure 5-2 of Bellcore GR-1244-CORE (refer to Figure G-1): less than 40 nanoseconds for observation times up to 1 second and less than 100 nanoseconds for times greater than 10 seconds. In determining this, the reference signal must be free of phase and frequency transients.

7. Pull-in or Acquisition Range

   Frequency range of the reference input signal over which the clock can successfully acquire the signal and achieve normal tracking.

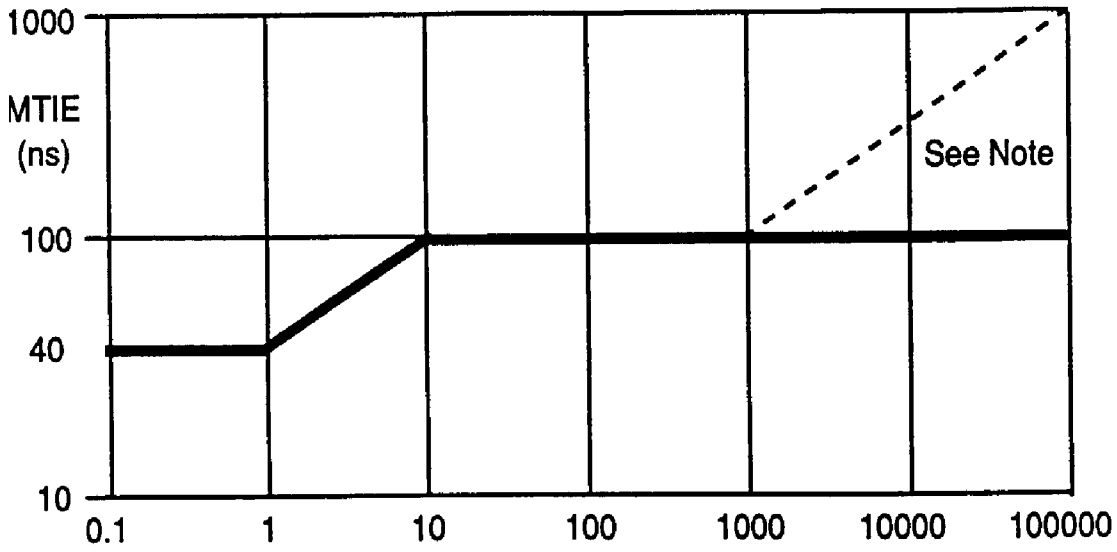
8. Rearrangement Requirement

   (Refer to Bellcore GR-1244-CORE, Section 3.4.)

   Specified MTIE and rate of change of phase occurring at the clock system output when switching between redundant track and hold cards. This is determined by circuitry on the output cards. Used in 5407 DS1 Output Driver Card. (Refer to Section 3, paragraph 3.37).

9. Settling Time

   Time interval from the beginning of an input phase offset or first entry into tracking to the time that normal tracking is achieved (refer to item 6). Prior to the input offset, normal tracking must have occurred for at least one settling time. An approximate rule of thumb is that the settling time is three (3) times the time constant.



Observation Time, S (seconds)	MTIE with limited temperature variations (nanoseconds)	MTIE with temperature variations per Section 10 (nanoseconds)
$S < 0.1$	N/A	N/A
$0.1 < S < 1$	40	40
$1 < S < 10$	40 x S^0.40	40 x S^0.40
$1 < S < 1000$	100	100
$1000 < S$	100	3.16 x S^0.5

NOTE: Basic mask is solid line curve which applies for limited temperature variations; for temperature variations to the limits established in Section 10 of Bellcore GR-1244-CORE, the solid line applies for observation times up to 1000 seconds and the dashed line applies above 1000 seconds.

Figure G-1. Wander Generation (MTIE)

10. Time Constant

    Time characterizing how fast a phase lock loop can respond to phase or frequency variations. The clock circuits are overdamped second order loops, which actually have two time constants but can be approximately described by a single time constant that is the reciprocal of the dominant pole of the closed loop response. In general terms, the clock circuit averages input variations occurring over a period of the order of several time constants. Because it is more easily and consistently measured, the time constant is used to estimate settling time.

11. Unit Interval

    Period of one bit: 488 nanoseconds for E1 (2.048 Mbps)
    648 nanoseconds for T1 (1.544 Mbps)

B. DS1 Signal Defects and Performance Parameters

1. Loss of Signal (LOS)

   Defined as 175 ± 75 consecutive zeroes. The LOS condition clears when the one's density is at least 12 1/2 percent during the 175 ± 75 bit intervals after the first 'one' following a LOS has occurred.

2. Out of Frame (OOF)

   Condition that occurs when any two out of five consecutive terminal framing bits contain errors in the framing pattern. The OOF condition clears when reframe occurs.

3. Loss of Frame (LOF)

   Term similar in meaning to OOF, above.

4. Time Interval Error (TIE)

   Variation in time delay of a given timing signal with respect to a reference timing signal over a specified time period. The variation is taken as the time delay at the end of the period minus the time delay at the beginning of the period.

5. Maximum Time Interval Error (MTIE)

   Limit for all possible intervals within a specified time period. This is calculated as the maximum time delay in the period minus the minimum time delay in the period.

6. Jitter

   Short-term variations of the significant instants (e.g. zero crossings) of a digital signal from their ideal positions in time. Short term implies phase variations occurring at rates greater than 10 Hz and less than 40 kHz.

7. Wander

   Long-term variations of the significant instants (e.g. zero crossings) of a digital signal from their ideal positions in time. Long term implies phase variations occurring at rates less than 10 Hz.

8. Slip

   Type of phase change. In the context of this document, a bit slip refers to a phase change of one bit time (648 nanoseconds) between a DS1 signal and a timing reference. A frame slip refers to a phase change of 193 bits (125 microseconds). The phase changes can take place over either a specified time period or an arbitrarily lengthy time period.